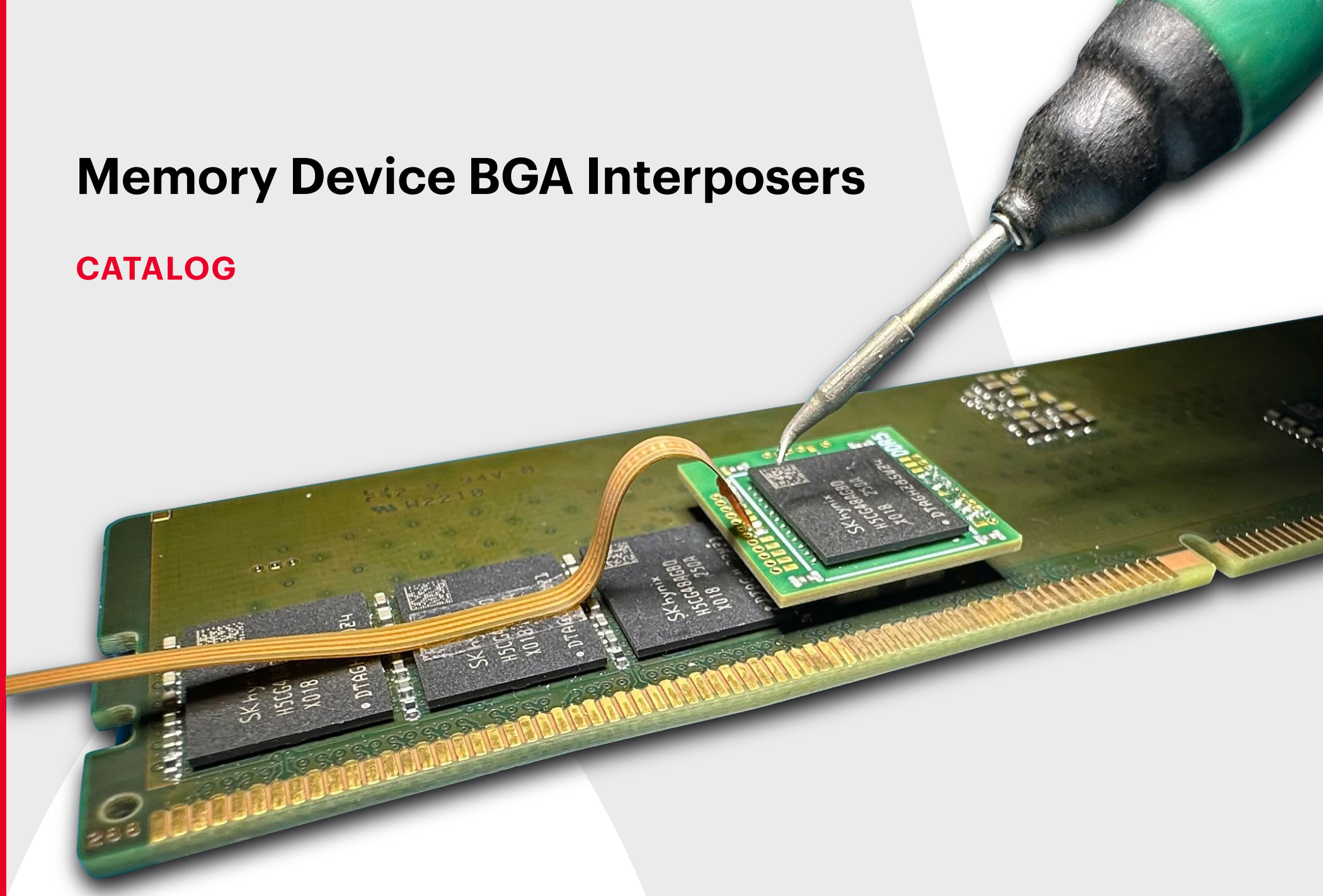
Memory Device BGA Interposers

CATALOG



KEYSIGHT

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Introduction

DIGITAL INTERPOSERS FOR MEMORY SYSTEM VALIDATION

Memory technology is constantly advancing in speed and density, and developers need probing solutions that can keep up with the changes. Make signal quality or protocol measurements with minimal effect on the system under test by positioning a ball grid array (BGA) interposer between the processor memory controller and the memory device. Interposers complement logic analyzers, oscilloscopes, and software for automated compliance, decoding, and protocol checking.

Choose from a large selection of existing interposer designs, or define probing solutions customized to your specific needs. Keysight's standard interposers are available for several Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association standard packages with a variety of ball counts. This catalog gives an overview of the interposers available and provides links to the corresponding data sheets.

For additional DRAM packages or to meet different mechanical requirements, Keysight's proven development process can produce custom BGA interposer designs of the highest quality.

Test directly

at the ball grid array of memory / processor systems

Optimize

measurements with an oscilloscope or logic analyzer

Customize

probing solutions for your specific needs

Design, test, and deliver your next breakthrough with our most advanced tools.

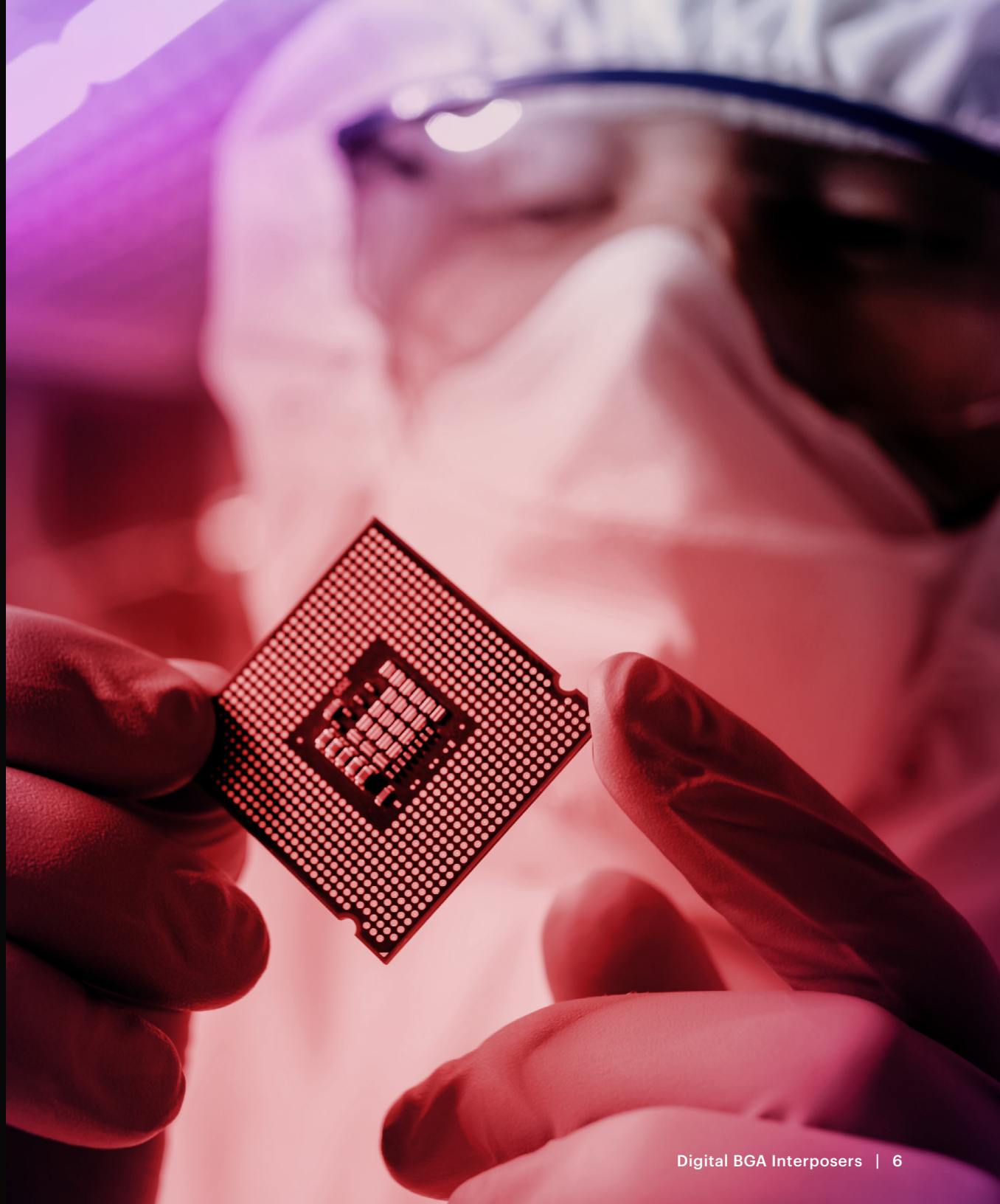
Keysight is at the forefront of the latest memory standards, chip technologies, and measurement techniques. Contact your local Keysight solution engineer for advice on a solution including measurement methodology, and probing techniques, and BGA interposer that best meets your application needs.

Interposers Matrix

Interposer	Standard	Ball count	DRAM type	DRAM size	Oscilloscope	Logic analyzer
DDR5 78 Signal Integrity Interposer	DDR5	78	x4/x8	9 mm x 12 mm	x	
DDR5 102 Signal Integrity Interposer	DDR5	102	x16	10 x 14 mm	x	
N2114A DDR4 BGA Interposers	DDR4	78	x4/x8	16 mm x 18 mm	x	
N2115A DDR4 BGA Interposers	DDR4	96	x16	12.5 mm x 19 mm	x	
W2635A DDR3 BGA Probe Adapter	DDR3	78	x4/x8	10 mm		
W2636A DDR3 BGA Probe Adapter	DDR3	96	x16	11 mm		
W5643A DDR5 x4/x8 78-ball BGA Interposer	DDR5	78	x4/x8	9 mm x 12 mm		x
DDR5 78 Trimline Logic Analyzer Interposer	DDR5	78	x4/x8	9 mm x 12 mm		x
DDR5 78 Clock Divider Logic Analyzer Interposer	DDR5	78	x4/x8	9 mm x 12 mm		x
DDR5 102 Trimline Logic Analyzer Interposer	DDR5	102	x16	10 x 14 mm		x
W4641A DDR4 x16 2-wing BGA Interposer	DDR4	96	x16	12.5 mm x 19 mm		x
W4636A DDR4 x16, 2-wing, small KOV BGA Interposer	DDR4	96	x16	12.5 mm x 19 mm		x
W4643A DDR4 x4/x8 BGA Interposer	DDR4	78	x4/x8	11 x 14 mm		x
W3631A DDR3 x16 BGA Command and Data Probe	DDR3	96	x16	-	x	x
W3633A DDR3 x4/x8 BGA Command and Data Probe	DDR3	78	x4/x8	-	x	x
W3636A DDR3 x16 Non-stacked DRAM BGA Interposer	DDR3	96	x16	-	x	x

Interposer	Standard	Ball count	DRAM type	DRAM size	Oscilloscope	Logic analyzer
W2633B DDR2 x8 BGA Command and Data Probe	DDR2	84	x8	-	x	x
W2631B DDR2 x16 BGA Command and Data Probe	DDR2	92	x16	-	x	x
LPDDR5 315 Signal Integrity Interposer	LPDDR5	315	2 X 32	15 mm x 12.4 mm	x	
LPDDR5 BGA 496 Signal Integrity Interposer	LPDDR5	496	Quad x16	20 mm x 12 mm	x	
LPDDR4/4x 200 Signal Integrity Interposer	LPDDR4/4x	200	2 X 16	10 mm x 15 mm	x	
LPDDR3 178 Signal Integrity Interposer	LPDDR3	178	x32	11.5 mm x 11 mm	x	
LPDDR5 315 Logic Analyzer Interposer	LPDDR5	315	2 X 32	15 mm x 12.4 mm		x
LPDDR4/4x 200 Logic Analyzer Interposer	LPDDR4/4x	200	2 X 16	10 mm x 15 mm		x
LPDDR4/4x 200 Rigid Logic Analyzer Interposer	LPDDR4/4x	200	1 X 32, 2 X 16	10 mm x 15 mm		x
LPDDR4 200 Logic Analyzer Interposer	LPDDR4	200	x32	10 mm x 15 mm		x
W3301A LPDDR3 178-ball BGA Interposer	LPDDR3	170	x32	13.5 mm x 13 mm		x
W2637A LPDDR BGA Probes	LPDDR2/3/4	60	x16	-	x	x
W2638A LPDDR BGA Probes	LPDDR2/3/4	90	x32	-	x	x
LPDDR2 121 Logic Analyzer Interposer	LPDDR2	121	x16	10 mm x 11 mm		x
GDDR5 170 Signal Integrity Interposer	GDDR5	170	-	12 mm x 14 mm	x	
eMMC 153 or 169 BGA Logic Analyzer Interposer	eMMC	153 or 169	-	11.5 mm x 13 mm		x

DDR Oscilloscope Interposers



DDR5 78 SIGNAL INTEGRITY INTERPOSER

Key features

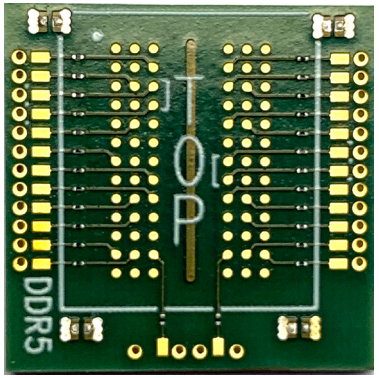
- The DDR5 high-performance signal integrity interposer is a rigid, 78-ball, DDR5 BGA interposer optimized for oscilloscope use. The interposer supports DDR5 8800+ with single channel, x8 DRAM chips.
- Probes a 78-ball DDR5 x8 DRAM chip, JESD79-5 footprint variation MO-210-AL, with a maximum chip package size of 9 x 12 mm.
- A DDR5 high-performance riser comes with the DDR5 high-performance signal integrity interposer kit for tight keep-out volume applications.
- Interposer and riser thicknesses are 1.0 mm and 1.9 mm, respectively.

Specifications

- Standard: DDR5
- Ball count: 78
- DRAM type: x4/x8
- DRAM size: 9 mm x 12 mm
- Optimized for oscilloscopes.

Requires

- Solder-in differential probe
- Heads
- InfiniiMax probe(s)
- Oscilloscope



	1	2	3	4	5	6	7	8	9	
A	LBDQ	GND	VPP				ZQ	GND	LBDQS	A
B	VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	B
C	GND	DQ0	DQS_t				DM_n	DQ1	GND	C
D	VDDQ	GND	DQS_c				TDQS_c	GND	VDDQ	D
E	VDD	DQ4	DQ6				DQ7	DQ5	VDD	E
F	GND	VDDQ	GND				GND	VDDQ	GND	F
G	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	G
H	ALERT_n	GND	CS_n				CK_c	GND	VDD	H
J	VDDQ	CA4	CA0				CA1	CA5	VDDQ	J
K	VDD	CA6	CA2				CA3	CA7	VDD	K
L	VDDQ	GND	CA8				CA9	GND	VDDQ	L
M	CAI	CA10	CA12				CA13	CA11	RESET_n	M
N	VDD	GND	VDD				VPP	GND	VDD	N
	1	2	3	4	5	6	7	8	9	

DDR5 102 SIGNAL INTEGRITY INTERPOSER

Key features

- The DDR5 High Performance Signal Integrity Interposer is a rigid, 102-ball, DDR5 BGA interposer optimized for oscilloscope use. This interposer supports DDR5 8800+ with single-channel, x16 DRAM chips.
- Probes a 102 ball DDR5 x16 DRAM chip, JEDEC JESD279-5 footprint variation MO-210-AT, with a maximum package size of 10 x 14 mm.
- For tight keep-out volume applications, the DDR5 High Performance Signal Integrity Interposer Kit includes a DDR5 High Performance Riser.
- Interposer and riser thicknesses are 1.0 mm and 1.9 mm, respectively.

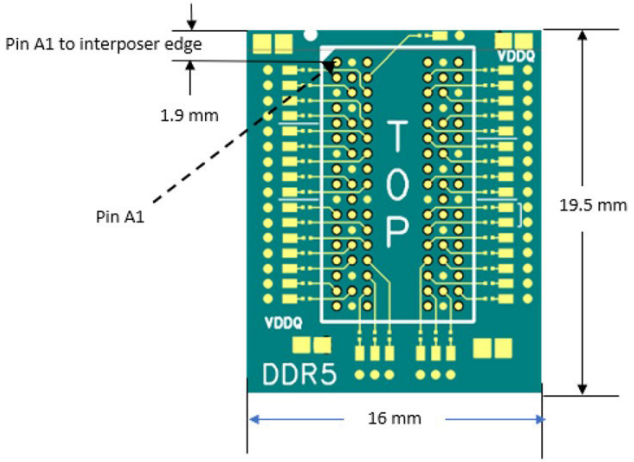
The DDR5 Interposer provides access to the signals highlighted below and passes all power and ground signals between the system and the memory chip. VDD and VDDQ power rails use separate power planes and power filter capacitor locations.

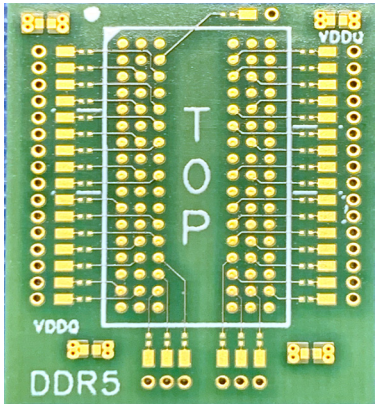
Specifications

- Standard: DDR5
- Ball count: 102
- DRAM type: x16
- DRAM size: 10 mm x 14 mm
- Optimized for oscilloscopes.

Requires

- Solder-in differential probe heads
- InfiniiMax probe(s)
- Oscilloscope





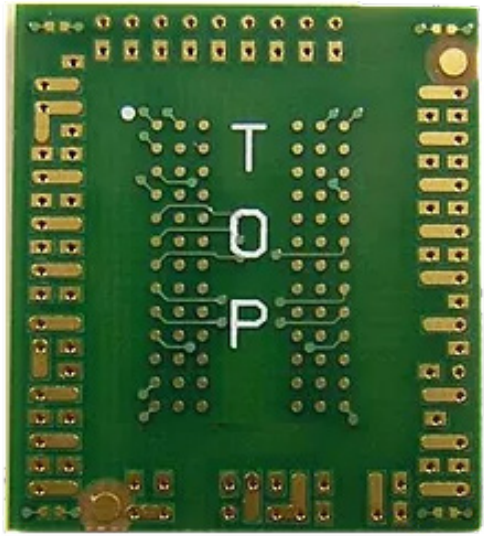
	1	2	3	4	5	6	7	8	9	
A	LBDQ	GND	VPP				ZQ	GND	LBDQS	A
B	VDD	VDDQ	DQU2				DQU3	VDDQ	VDD	B
C	GND	DQU0	DQSU_t				DMU_n	DQU1	GND	C
D	VDDQ	GND	DQSU_c				RFU	GND	VDDQ	D
E	VDD	DQU4	DQU6				DQU7	DQU5	VDD	E
F	GND	VDDQ	DQL2				DQL_3	VDDQ	GND	F
G	GND	DQL0	DQSL_t				DML_n	DQL1	GND	G
H	VDDQ	GND	DQSL_c				RFU	GND	VDDQ	H
J	VDD	DQL4	DQL6				DQL7	DQL5	VDD	J
K	GND	VDDQ	GND				GND	VDDQ	GND	K
L	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	L
M	ALERT_n	GND	CS_n				CK_c	GND	VDD	M
N	VDDQ	CA4	CA0				CA1	CA5	VDDQ	N
P	VDD	CA6	CA2				CA3	CA7	VDD	P
R	VDDQ	GND	CA8				CA9	GND	VDDQ	R
T	CAI	CA10	CA12				CA13	CA11	RESET_n	T
U	VDD	GND	VDD				VPP	GND	VDD	U
	1	2	3	4	5	6	7	8	9	

N2114A DDR4 BGA INTERPOSERS (DRAM X4/X8)

Key features

- Provides signal access points for DDR4 DRAM x4/x8 packages using JEDEC-standard common BGA footprints to the oscilloscope.
- Perimeter solder-down test points can be used with logic analyzer flying leads or oscilloscope solder-down probe tips to access signals.
- Extend effective bandwidth with InfiniiSim software.
- Reduce measurement timing skews by matched trace lengths from DDR4 balls to test points.
- S-parameter models are available for use with InfiniiSim for de-embedding purposes.
- The N2114A DDR4 BGA interposers provide signal access to the clock, strobe, data, address, and command signals of the DDR4 BGA package for making electrical and timing measurements with an Infiniium oscilloscope. With the DDR4 JEDEC specification defined at the DRAM ballout, the BGA probe adapter provides direct signal access to the BGA package for true compliance testing.

N2114A DDR4 BGA interposers should be soldered in between the DRAM and PC board or DIMM raw card where the DRAM would normally be soldered. These interposers are designed with the PCB or DIMM footprint on the bottom side and the DRAM footprint on the top side. The signals from the memory controller chip and DRAM pass directly to the top side of the BGA probe adapter, where they can be accessed with the oscilloscope probes.



Specifications

- Standard: DDR4
- Ball count: 78
- DRAM type: x4/x8
- DRAM size: 16 mm x 18 mm
- Optimized for oscilloscopes

Requires

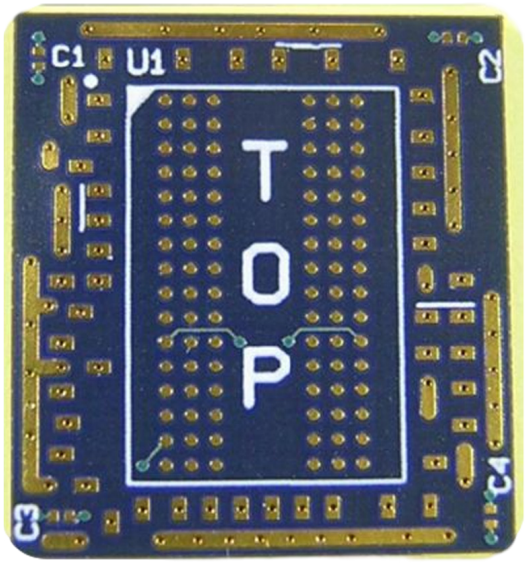
- Solder-in differential probe heads
- InfiniiMax probe(s)
- Oscilloscope

N2115A DDR4 BGA INTERPOSERS (DRAM X16)

Key features

- Provides signal access points for DDR4 DRAM x16 packages using JEDEC-standard common BGA footprints to the oscilloscope.
- Perimeter solder-down test points can be used with logic analyzer flying leads or oscilloscope solder-down probe tips to access signals.
- Extend effective bandwidth with InfiniiSim software.
- Reduce measurement timing skews by matched trace lengths from DDR4 balls to test points.
- Probing compatibility with InfiniiMax probes with differential solder-in probe heads.
- S-parameter models are available for use with InfiniiSim for de-embedding purposes.

The N2115A DDR4 BGA Interposers are soldered in between the DRAM and PC board or DIMM raw card where the DRAM would normally be soldered. They are designed with the PCB or DIMM footprint on the bottom side and the DRAM footprint on the top side. The signals from the memory controller chip and DRAM then pass directly to the top side of the BGA probe adapter, where they can be accessed with the oscilloscope probes.



Specifications

- Standard: DDR4
- Ball count: 96
- DRAM type: x16
- DRAM size: 12.5 mm x 19 mm
- Optimized for oscilloscopes

Requires

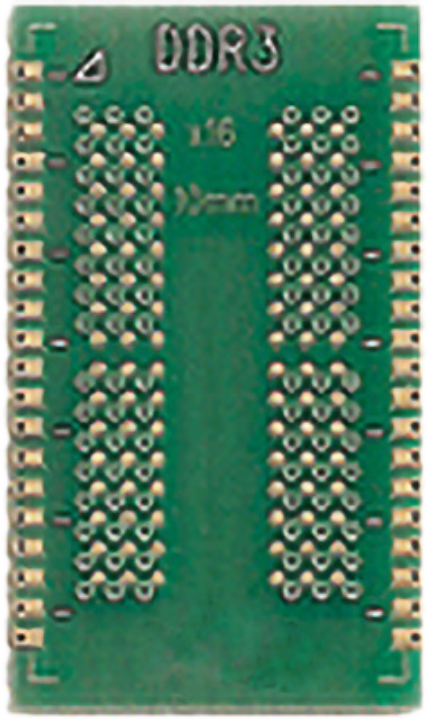
- Solder-in differential probe heads
- InfiniiMax probe(s)
- Oscilloscope

W2635A DDR3 BGA PROBE ADAPTER (X8)

Key features

- The adapters provide signal access points for DDR3 DRAM x4/x8 packages using JEDEC-standard common BGA footprints to the oscilloscope (JESD79-3A).
- The BGA probe adapter width is 10 mm.
- Buried resistors provide signal isolation and minimize capacitive loading.

The W2635A DDR3 BGA probe adapters are soldered in between the DRAM and the PC board or DIMM raw card where the DRAM would normally be soldered. They are designed with the PCB or DIMM footprint on the bottom and the DRAM footprint on the top. The signals from the memory controller chip and DRAM then pass directly to the top of the BGA probe adapter, where they are accessible with the oscilloscope probes.



Specifications

- Standard: DDR3
- Ball count: 78
- DRAM size: x4/x8
- Optimized for oscilloscopes

Requires

- Solder-in differential probe heads
- InfiniiMax probe(s)
- Oscilloscope

W2636A DDR3 BGA PROBE ADAPTER (X16)

Key features

- The adapters provide signal access points for DDR3 DRAM x16 packages using JEDEC standard common BGA footprints to the oscilloscope.
- The adapters have an 11 mm BGA probe adapter width.
- Buried resistors provide signal isolation and minimize capacitive loading.

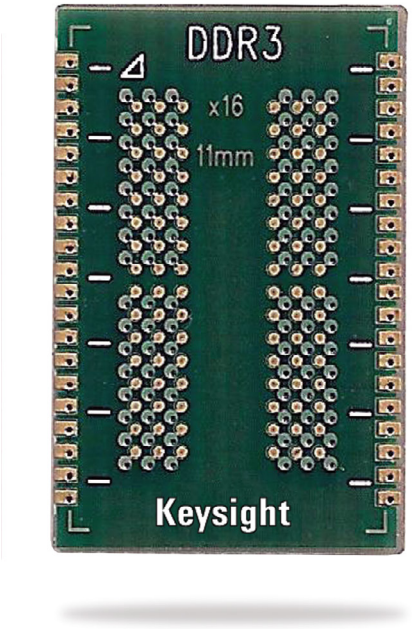
W2636A DDR3 x16 BGA probe adapters are soldered in between the DRAM and the PC board or DIMM raw card where the DRAM would normally be soldered. They are designed with the PCB or DIMM footprint on the bottom and the DRAM footprint on the top. The signals from the memory controller chip and DRAM pass directly to the top of the BGA probe adapter, where they are accessible with the oscilloscope probes.

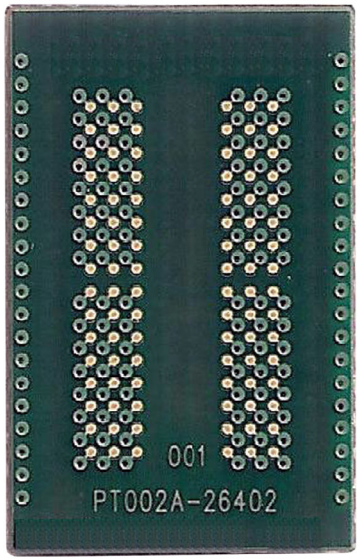
Specifications

- Standard: DDR3
- Ball count: 96
- DRAM size: x16
- Optimized for oscilloscopes

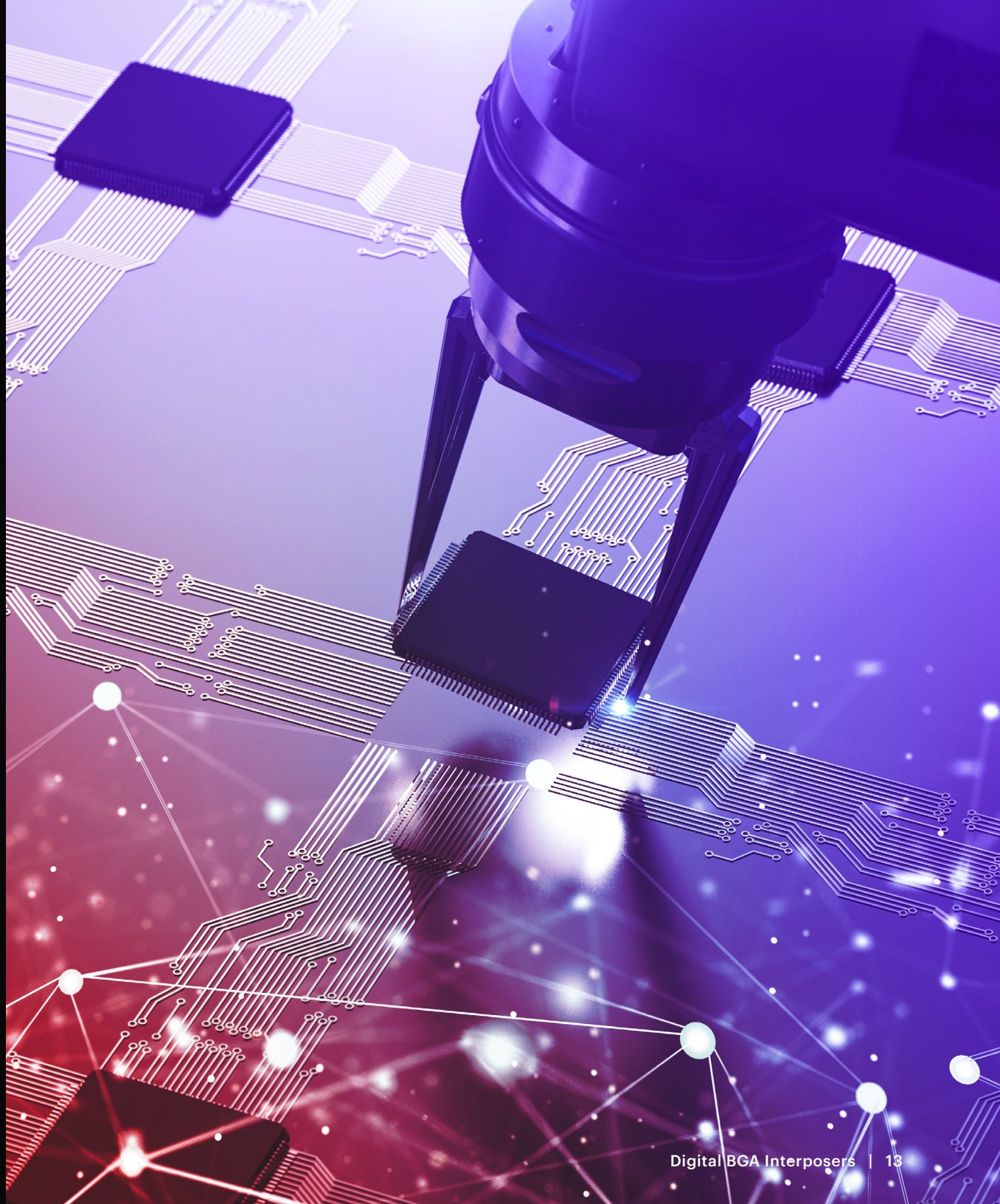
Requires

- Solder-in differential probe heads
- InfiniiMax probe(s)
- Oscilloscope





DDR Logic Analyzer Interposers



W5643A DDR5 X4/X8 78-BALL BGA INTERPOSER

Key features

- Achieves protocol decode for up to 5GT/s DDR5 data rates and data capture up to 4GT/s when used with a U4164A logic analyzer system with speed option U4164A-02G. Provides a connection to all (address, command, control, and data) signals between a U4164A logic analysis system and JEDEC-standard 78 ball DDR5 x4/x8 DRAM.
- Enables observation of data traffic on industry-standard 78-ball DDR5 x4/x8 DRAM and provides access for DDR eye scans and burst scans of DDR5 signals.
- The W5643A ships with a custom 78-ball DDR5 riser to provide clearance for surrounding devices. The riser can be replaced with an optional third-party socket (not provided).
- Works with all solder finishes and is designed to tolerate lead-free soldering temperature profiles.

The W5643A DDR5 x4/x8 BGA interposer enables signal access to the DDR5 signals critical to your debug and validation effort through a U4164A logic analyzer. The probe works in existing designs and eliminates the need for upfront planning or redesign. The probe connects directly to the balls of the DRAM or can be installed with a DDR5 78 ball riser (included) or an optional third-party socket (not provided), enabling the operation and acquisition of high-speed DDR5 signals.

	1	2	3	4	5	6	7	8	9	
A	LBDQ	GND	VPP				ZQ	GND	LBDQS	A
B	VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	B
C	GND	DQ0	DQS_t				DM_n	DQ1	GND	C
D	VDDQ	GND	DQS_c				TDQS_c	GND	VDDQ	D
E	VDD	DQ4	DQ6				DQ7	DQ5	VDD	E
F	GND	VDDQ	GND				GND	VDDQ	GND	F
G	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	G
H	ALERT_n	GND	CS_n				CK_c	GND	VDD	H
J	VDDQ	CA4	CA0				CA1	CA5	VDDQ	J
K	VDD	CA6	CA2				CA3	CA7	VDD	K
L	VDDQ	GND	CA8				CA9	GND	VDDQ	L
M	CAI	CA10	CA12				CA13	CA11	RESET_n	M
N	VDD	GND	VDD				VPP	GND	VDD	N
	1	2	3	4	5	6	7	8	9	

Specifications

- Standard: DDR5
- Ball count: 78
- DRAM type: x4/x8
- DRAM size: 9 mm x 12 mm
- Optimized for logic analyzers

Each W5643A includes:

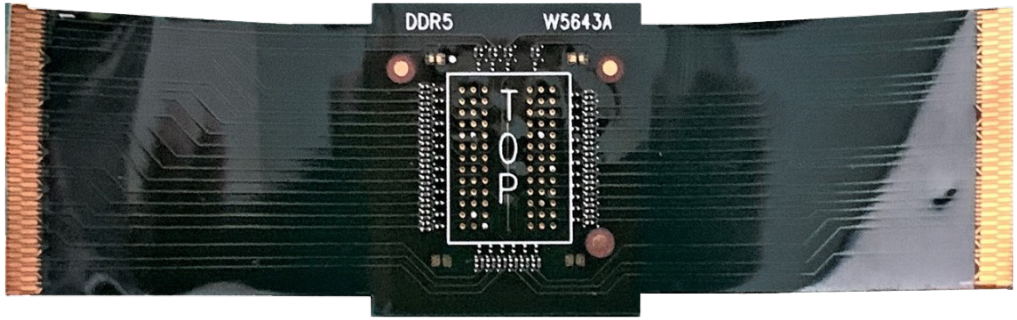
- DDR5 x4/x8 78-ball BGA interposer
- DDR5 x4/x8 78-ball BGA riser

Each W5643A requires:

- Qty (1) U4164A logic analyzer module with option-02G for quad sample state mode
- Chassis for U4164A logic analyzer module(s) with controller or host PC
- Qty (1) U4208A probe / cable, 61-pin ZIF, no RC, 160-pin direct connect
- Qty (1) U4209A probe / cable, 61-pin ZIF, no RC, 160-pin direct connect
- B4661A Memory Analysis software (base software for DDR Setup Assistant and default configurations)

Recommended

- Qty (1) B4661A-5FP / -5TP / -5NP DDR5 analysis and compliance software. Licensed option for rapid navigation, debugging, and validation of DDR5 protocol
- Memory depth option of choice for the U4164A logic analyzer module



DDR5 78 TRIMLINE LOGIC ANALYZER INTERPOSER

Key features

- Pin1 is offset to one edge of the interposer to allow for optimal fit into systems under test that have tight keep-out volume (KOV) on the pin 1 edge of the DRAM.
- Achieves protocol decode for up to 5GT/s DDR5 data rates and data capture up to 4GT/s when used with a U4164A logic analyzer system with speed option U4164A-02G. Provides a connection to all (address, command, control, and data) signals between a U4164A logic analysis system and JEDEC-standard 78 ball DDR5 x4/x8 DRAM.
- Provides observation of data traffic on industry-standard 78-ball DDR5 x4/x8 DRAM and provides access for DDR eye scans and burst scans of DDR5 signals.
- Ships with a custom 78-ball DDR5 riser to provide clearance for surrounding devices. Riser can be replaced with an optional third-party socket (not provided).
- Works with all solder finishes and is designed to tolerate lead-free soldering temperature profiles.
- Interposer and riser thicknesses are 0.5 mm and 1.9 mm, respectively.

Specifications

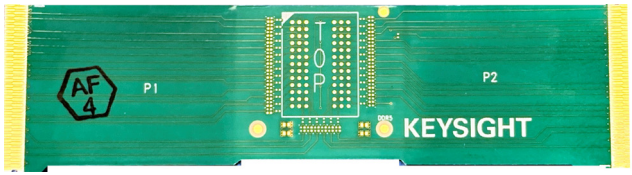
- Standard: DDR5
- Ball count: 78
- DRAM type: x4/x8
- DRAM size: 9 mm x 12 mm
- Optimized for logic analyzers
- Each trimline includes:
- DDR5 x4/x8 78-ball BGA interposer
- DDR5 x4/x8 78-ball BGA riser

Requires

- Qty (1) U4164A logic analyzer module with Option -02G for quad sample state mode
- Chassis for U4164A logic analyzer module(s) with controller or host PC
- Qty (1) U4208A probe / cable, 61-pin ZIF, no RC, 160-pin direct connect
- Qty (1) U4209A probe / cable, 61-pin ZIF, no RC, 160-pin direct connect
- B4661A Memory Analysis software (base SW for DDR Setup Assistant and default configurations)

Recommended

- B4661A Memory Analysis software licensed option:
  - Qty (1) B4661A-5FP / -5TP / -5NP
- DDR5 Analysis and Compliance software
- Memory depth option of choice for the U4164A logic analyzer module



DDR5 78 CLOCK DIVIDER LOGIC ANALYZER INTERPOSER

Key features

- DDR5 data rates up to 8GT/s.
- The A9-LGC-45-BLF, DDR5 x4/x8 BGA 78 Clock Divider Interposer enables viewing of DDR5 command / address traffic on industry standard DDR5 x4/x8,78-ball DRAMs operating at data rates up to 8000 MT/s.
- Provides observability of all command / address signals between a U4164A logic analysis system DDR5 x4/x8 DRAM.
- For tight keep-out volume applications, the Clock Divider Interposer DDR5 Logic Analysis Interposer is designed to minimize the clearance required between interposed DRAM pin A1 and the interposer edge. The DDR5 logic analysis interposer kit includes a riser to elevate the interposer above the surrounding components.

The DDR5 78-ball BGA Clock Divider interposers for the Keysight U4164A logic analysis systems, enable viewing of DDR5 command / address (CA) traffic on industry standard DDR5 x4/x8, 78-ball DRAMs operating at data rates up to 8000 MT/s.

Specifications

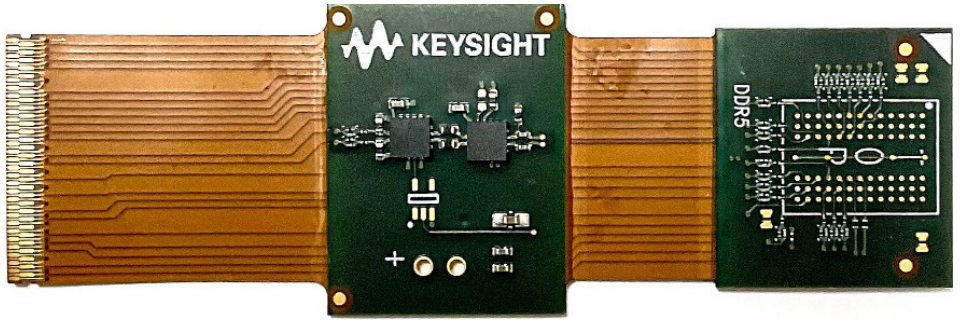
- Standard: DDR5
- Ball count: 78
- DRAM type: x4/x8
- DRAM size: 9 mm x 12 mm
- Optimized for logic analyzers

Requires

- External 3.3V supply
- Qty (1) U4164A logic analyzer module with option -02G for quad sample state mode
- Chassis for U4164A logic analyzer module(s) with controller or host PC
- Qty (1) U4208A probe/cable, 61-pin ZIF, 160-pin direct connect to logic analyzer front panel connector.
- B4661A Memory Analysis software (base software for DDR Setup Assistant and default configurations)

Recommended

- Qty (1) B4661A-5FP / -5TP / -5NP DDR5 Analysis and Compliance software
- Memory depth option of choice for the U4164A logic analyzer module



DDR5 102 TRIMLINE LOGIC ANALYZER INTERPOSER

Key features

- Pin1 is offset to one edge of the interposer to allow for optimal fit into systems under test that have tight keep-out volume (KOV) on the pin 1 edge of the DRAM.
- Achieves protocol decode for up to 5GT/s DDR5 data rates and data capture up to 4GT/s when used with a U4164A logic analyzer system with speed option U4164A-02G. Provides a connection to all (address, command, control, and data) signals between a U4164A logic analysis system and JEDEC-standard 102 ball DDR5 x16 DRAM.
- Provides connection to all (address, command, control, and data) signals between a U4164A logic analysis system and JEDEC-standard 102 ball DDR5 x16 DRAM).
- Provides observation traffic on industry-standard 102-ball DDR5 x16 DRAM and access for DDR eye scans of DDR5 signals.
- The Interposer ships with a custom 102-ball DDR5 riser to provide clearance for surrounding devices.
- Interposer and riser thicknesses are 1.5 mm and 2.0 mm, respectively.

DDR5 102-ball BGA interposers for logic analyzers enable viewing of DDR5 traffic on industry-standard DDR5 x16 DRAMs with the Keysight U4164A logic analysis systems.

Specifications

- Standard: DDR5
- Ball count: 102
- DRAM type: x16
- DRAM size: 10 mm x 14 mm
- Optimized for logic analyzers

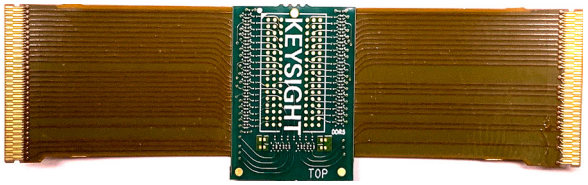
	1	2	3	4	5	6	7	8	9	
A	LBDQ	GND	VPP				ZQ	GND	LBDQS	A
B	VDD	VDDQ	DQU2				DQU3	VDDQ	VDD	B
C	GND	DQU0	DQSU_t				DMU_n	DQU1	GND	C
D	VDDQ	GND	DQSU_c				RFU	GND	VDDQ	D
E	VDD	DQU4	DQU6				DQU7	DQU5	VDD	E
F	GND	VDDQ	DQL2				DQL_3	VDDQ	GND	F
G	GND	DQL0	DQSL_t				DML_n	DQL1	GND	G
H	VDDQ	GND	DQSL_c				RFU	GND	VDDQ	H
J	VDD	DQL4	DQL6				DQL7	DQL5	VDD	J
K	GND	VDDQ	GND				GND	VDDQ	GND	K
L	CA_ODT	MIR	VDD				CK_t	VDDQ	TEN	L
M	ALERT_n	GND	CS_n				CK_c	GND	VDD	M
N	VDDQ	CA4	CA0				CA1	CA5	VDDQ	N
P	VDD	CA6	CA2				CA3	CA7	VDD	P
R	VDDQ	GND	CA8				CA9	GND	VDDQ	R
T	CAI	CA10	CA12				CA13	CA11	RESET_n	T
U	VDD	GND	VDD				VPP	GND	VDD	U
	1	2	3	4	5	6	7	8	9	

Requires

- Qty (1) U4164A logic analyzer module with Option -02G for quad sample state mode
- Chassis for U4164A logic analyzer module(s) with controller or host PC
- Qty (1) U4208A probe / cable, 61-pin ZIF, no RC, 160-pin direct connect.
- Qty (1) U4209A probe / cable, 61-pin ZIF, no RC, 160-pin direct connect.
- B4661A Memory Analysis software (base software for DDR Setup Assistant and default configurations)

Recommended

- Qty (1) B4661A-5FP / -5TP / -5NP DDR5 Analysis and Compliance software
- Memory depth option of choice for the U4164A logic analyzer module



W4641A DDR4 X16 2-WING BGA INTERPOSER

Key features

- Industry's smallest DDR4 x16 BGA interposer, designed to exceed 3.2 Gb/s data rates. Provides connection to all (address, command, control, and data) signals between a U4164A logic analysis system and JEDEC- standard 96-ball DDR4 x16 DRAM.
- Provides observation of data traffic on industry-standard 96-ball DDR4 x16 DRAM and access for DDR eye scans and burst scans of DDR4 signals.
- The W4641A ships with a custom 96-ball DDR4 riser, required for keep-out volume (KOV) under the interposer (riser can be replaced with optional 3rd party socket –not provided)
- Works with all solder finishes and is designed to tolerate lead-free soldering temperature profiles.

The W4641A DDR4 2-wing BGA interposer for DDR4 x16 BGA DRAM probing takes full advantage of the quad sample state mode on the U4164A. The W4641A is the smallest BGA interposer for DDR4 x16 DRAM, capable of capturing simultaneous read and write traffic at data rates exceeding 3.2 Gb/s. U4208A and U4209A probe / cables connect any W4640A Series DDR4 BGA interposer directly into the U4164A logic analyzer module from 61-ball, high-density zero insertion force (ZIF) connectors that attach to the W4640A Series BGA interposer wings.

	1	2	3	4	5	6	7	8	9	
A	VDDQ	GND	DQU0				DQSU_c	GND	VDDQ	A
B	VPP	GND	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	GND	C
D	VDD	GND	DQU6				DQU7	GND	VDDQ	D
E	GND	DMU_n	GND				DML_n	GND	GND	E
F	GND	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	GND	VDDQ	G
H	GND	DQL4	DQL2				DQL3	DQL5	GND	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	GND	CKE	ODT				CK_t	CK_c	GND	K
L	VDD	A14/ WE_n	ACT_n				CS_n	A16/ RAS_n	VDD	L
M	VREFCA	BG0	A10/ AP				A12/ BC_n	A15/ CAS_n	GND	M
N	GND	BA0	A4				A3	BA1	TEN	N
P	RST_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	GND	A11	PAR				NC	A13	VDD	T
	1	2	3	4	5	6	7	8	9	

Specifications

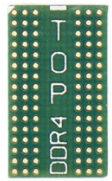
- Standard: DDR4
- Ball count: 96
- DRAM type: x16
- DRAM size: 12.5 mm x 19 mm
- Optimized for logic analyzers

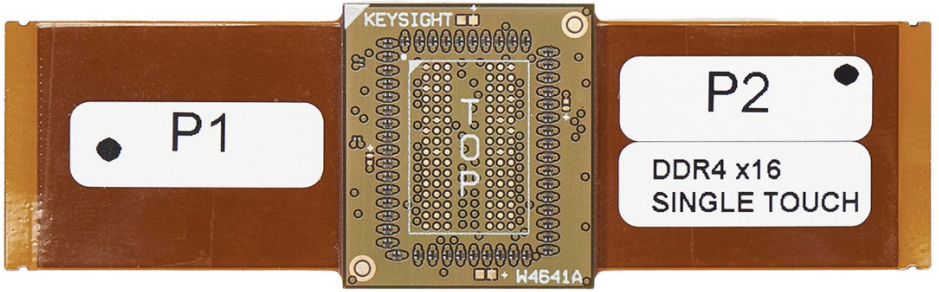
Requires

- U4164A logic analyzer module with option -02G for quad sample state mode
- Chassis for U4164A logic analyzer module(s) with controller or host PC
- Qty (1) U4208A probe / cable, 61-pin ZIF, 160-pin direct connect to logic analyzer front panel connector
- Qty (1) U4209A probe / cable, 61-pin ZIF, 160-pin direct connect to logic analyzer front panel connector
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module





W4636A DDR4 X16, 2-WING, SMALL KOV, BGA INTERPOSER

The W4636A DDR4 x16, two-wing BGA interposer for 96-ball DDR4 DRAM is designed for data rates up to and including 2.4 Gb/s. The W4636A probes all ADD / CMD / CNTRL and partial DQ / DQS, and it is designed for minimal KOV for space-limited systems under test. The W4636A is the least expensive DDR4 BGA interposer for a logic analyzer.

Key features

- Provides connection to all (address, command, and control) and partial DQ (data signals) between a U4164A logic analysis system and JEDEC-standard 96 ball DDR4 x16 DRAM (JEDEC MO-207 footprint variation DU-z).
- Provides observation of probed signals on industry-standard 96 ball DDR4 x16 DRAM and provides access for DDR eye scans of DDR4 signals.
- Works with all solder finishes and is designed to tolerate lead-free soldering temperature profiles.
- Designed for the smallest KOV for a DDR4 x16 96 ball BGA interposer, and the two-wing design allows capture of data rates up to and including 2400 Mb/s.

	1	2	3	4	5	6	7	8	9	
A	VDDQ	GND	DQU0				DQSU_c	GND	VDDQ	A
B	VPP	GND	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	GND	C
D	VDD	GND	DQU6				DQU7	GND	VDDQ	D
E	GND	DMU_n	GND				DML_n	GND	GND	E
F	GND	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	GND	VDDQ	G
H	GND	DQL4	DQL2				DQL3	DQL5	GND	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	GND	CKE	ODT				CK_t	CK_c	GND	K
L	VDD	A14	ACT_n				CS_n	A16	VDD	L
M	VREFCA	BG0	A10				A12	A15	GND	M
N	GND	BA0	A4				A3	BA1	TEN	N
P	RST_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	GND	A11	PAR				NC	A13	VDD	T
	1	2	3	4	5	6	7	8	9	

Specifications

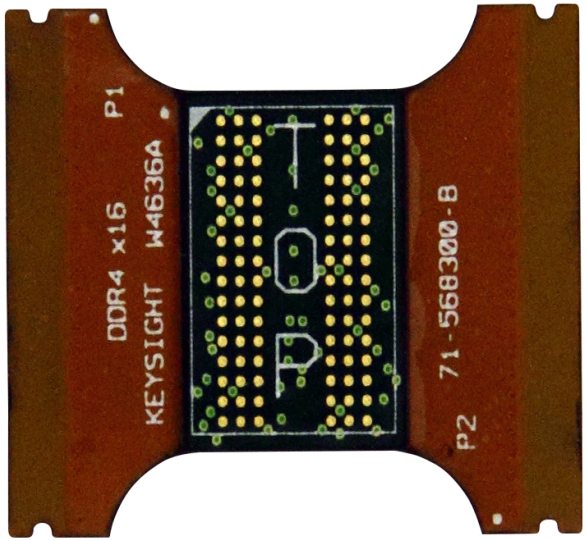
- Standard: DDR4
- Ball count: 96
- DRAM type: x16
- DRAM size: 12.5 mm x 19 mm
- Optimized for logic analyzers

Requires

- Qty (1) E5847A ZIF probe
- Qty (1) U4164A logic analyzer module with option -02G
- Qty (3) U4201A logic analyzer cables
- Chassis for U4164A logic analyzer(s) with controller or host PC

Recommended

- B4661A Memory Analysis software and license options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module



W4643A DDR4 x4/x8 BGA interposer

Key features

- The industry's smallest DDR4 x4/x8 BGA interposer, designed to exceed 3.2 Gb/s data rates. Provides connection to all (address, command, control, and data) signals between a U4164A logic analysis system and JEDEC-standard 78 ball DDR4 x4/x8 DRAM).
- Provides observation of data traffic on industry-standard 78-ball DDR4 x4/x8 DRAM and provides access for DDR eye scans and burst scans of DDR4 signals.
- W4641A ships with a custom 78-ball DDR4 riser, required for KOV under the interposer. The riser can be replaced with an optional third-party socket (not provided). Works with all solder finishes and is designed to tolerate lead-free soldering temperature profiles.

The W4643A DDR4 x4/x8 BGA interposer enables signal access to the DDR4 signals critical to your debug and validation effort through a U4164A logic analyzer. The probe works in existing designs and eliminates the need for up-front planning or redesign. The probe connects directly to the balls of the DRAM or can be installed with a DDR4 78 ball riser (included) or an optional third-party socket (not provided), enabling the operation and acquisition of high-speed DDR4 signals.

	1	2	3	4	5	6	7	8	9	
A	VDD	GND	TDQS_c				DBI_n	GND	GND	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	GND	VDDQ	C
D	GND	DQ4	DQ2				DQ3	DQ5	GND	D
E	GND	VDDQ	DQ6				DQ7	VDDQ	GND	E
F	VDD	C2	ODT				CK_t	CK_c	VDDQ	F
G	GND	C0	CKE				CS_n	C1	TEN	G
H	VDD	A14	ACT_n				A15	A16	GND	H
J	VrefCA	BG0	A10				A12	BG1	VDDQ	J
K	GND	BA0	A4				A3	BA1	GND	K
L	RST_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	GND	A11	PAR				A17	A13	VDDQ	N
	1	2	3	4	5	6	7	8	9	

Specifications

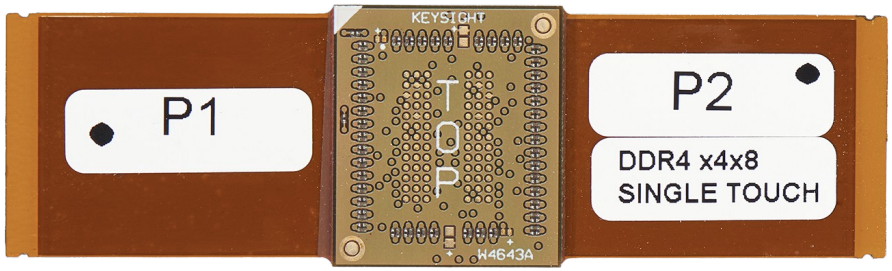
- Standard: DDR4
- Ball count: 78
- DRAM type: x4/x8
- DRAM size: 11 mm x 14 mm
- Optimized for logic analyzers

Requires

- U4164A logic analyzer module with option -02G for quad sample state mode
- Chassis for U4164A logic analyzer module(s) with controller or host PC
- Qty 1 U4208A probe/cable, 61-Ball ZIF, 160-pin direct connect to logic analyzer front panel connector
- Qty 1 U4209A probe/cable, 61-pin ZIF, 160-pin direct connect to logic analyzer front panel connector
- B4661A Memory Analysis SW

Recommended

- B4661A Memory Analysis software license options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module



W3631A DDR3 X16 BGA COMMAND AND DATA PROBE

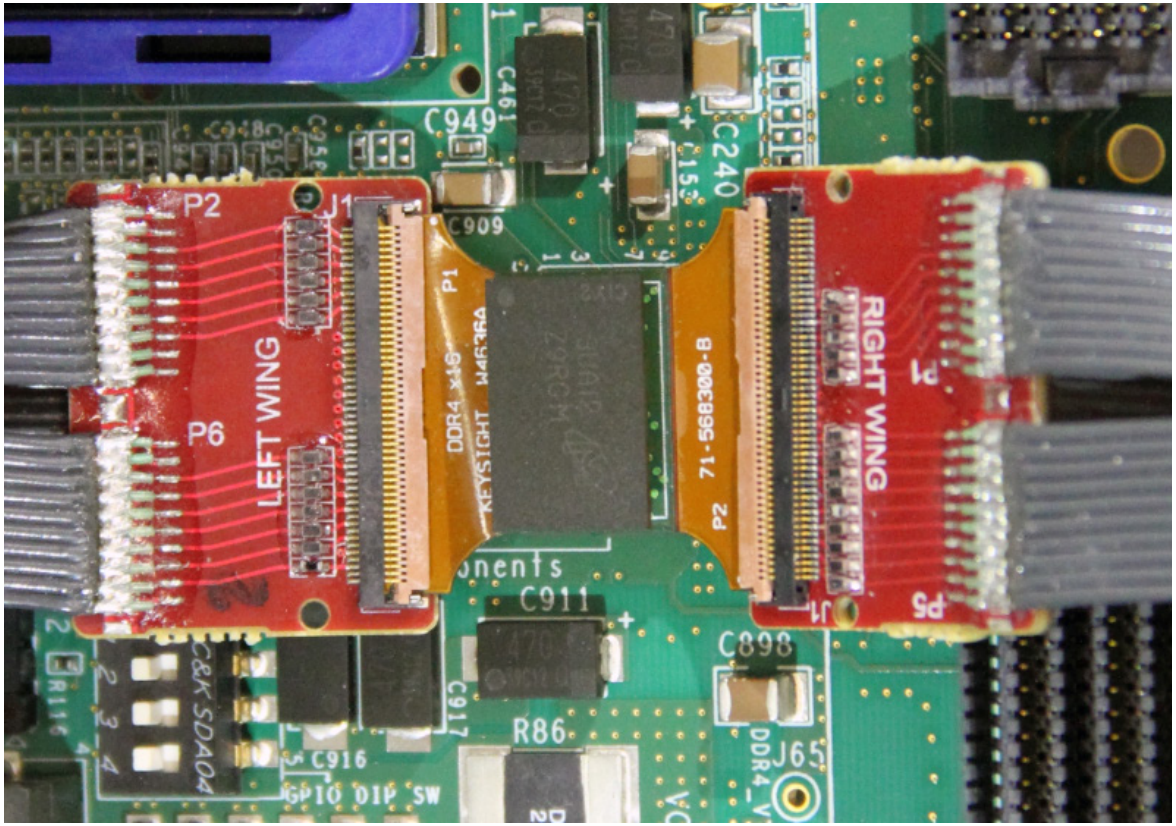
Key features

- Provides an electrically and mechanically non-intrusive connection to all signals (address, command, control, and 16 bits of data) between a U4164A or 16864A Series logic analysis system and DDR3 DRAMs.
- Provides access to representative signals for scope measurement of compliance to the JEDEC specification.
- Provides observation of data traffic on industry-standard DDR3 DIMMs. Works with all solder finishes. Designed to tolerate lead-free soldering temperature profiles.

The W3631A DDR3 BGA probe enables you to get complete signal access to the DDR3 signals critical to your debug and validation effort through a logic analyzer. The probe works in existing designs and eliminates the need for upfront planning or re-design. The probe connects directly to the balls of the DRAM, enabling you to operate at full speed and acquire high-speed DDR3 signals without impacting the performance of your logic design.

Specifications

- Standard: DDR3
- Ball count: 96
- DRAM type: x16



Use with oscilloscope requires

- W3635A scope probe adapter(s)
- E2678B socketed probe head(s)
- Oscilloscope probe(s)
- Oscilloscope

Use with logic analyzer requires

- Qty (1) E5845A ZIF probe
- Qty (1) U4164A module in AXIe chassis or 16864A logic analyzer
- Qty (2) U4201A logic analyzer cables
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable, required for U4164A solution
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4 LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module with minimum of U4164A-01G speed grade option

W3633A DDR3 X4/X8 BGA COMMAND AND DATA PROBE

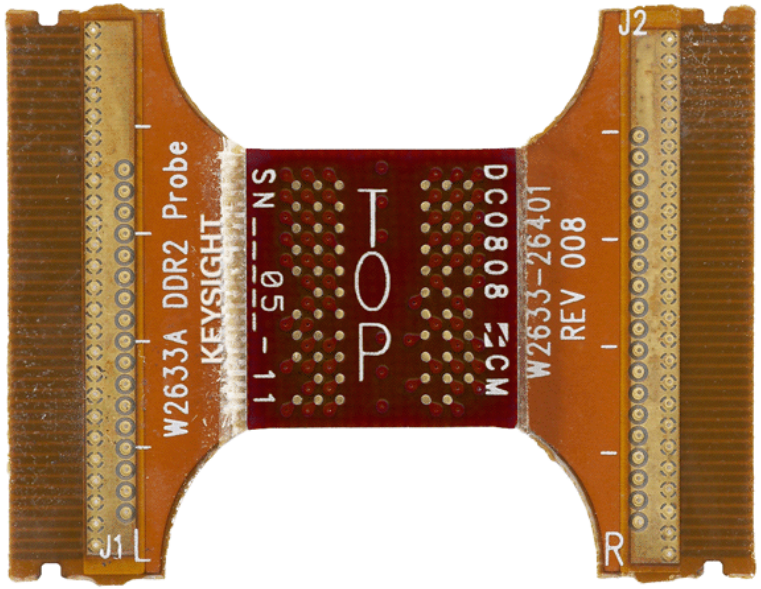
Key features

- Provides an electrically and mechanically non-intrusive connection to all signals (address, command, control, and 4 or 8 bits of data) between a U4164A or 16846A Series logic analysis system and DDR3 DRAMs.
- Provides access to representative signals for scope measurement of compliance with the JEDEC specification.
- Provides observation of data traffic on industry-standard DDR3 DRAM. Works with all solder finishes. Designed to tolerate lead-free soldering temperature profiles.

The W3633A DDR3 BGA probe enables you to get complete signal access to the DDR3 signals critical to your debug and validation effort. The probe works in existing designs and eliminates the need for upfront planning or re-design. The probe connects directly to the balls of the DRAM, enabling you to operate at full speed and acquire high-speed DDR3 signals without impacting the performance of your design.

Specifications

- Standard: DDR3
- Ball count: 78
- DRAM type: x4x8
- Optimized for oscilloscopes and logic analyzers



Key features

- Provides an electrically and mechanically non-intrusive connection to all signals (address, command, control, and 4 or 8 bits of data) between a U4164A or 16846A Series logic analysis system and DDR3 DRAMs.
- Provides access to representative signals for scope measurement of compliance with the JEDEC specification.
- Provides observation of data traffic on industry-standard DDR3 DRAM. Works with all solder finishes. Designed to tolerate lead-free soldering temperature profiles.

Use with oscilloscope requires:

- W3635A scope probe adapter(s)
- E2678B socketed probe head(s)
- Oscilloscope probe(s)
- Oscilloscope

Use with logic analyzer requires

- Qty (1) E5847A ZIF probe
- Qty (2) U4201A logic analyzer cables
- Qty (1) U4164A module in AXIe chassis or 16864A logic analyzer
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable, required for U4164A solution
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4 AND LPDDR2/3/4 ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module with minimum of U4164A-01G speed grade option

W3636A DDR3 X16 NON-STACKED DRAM BGA INTERPOSER

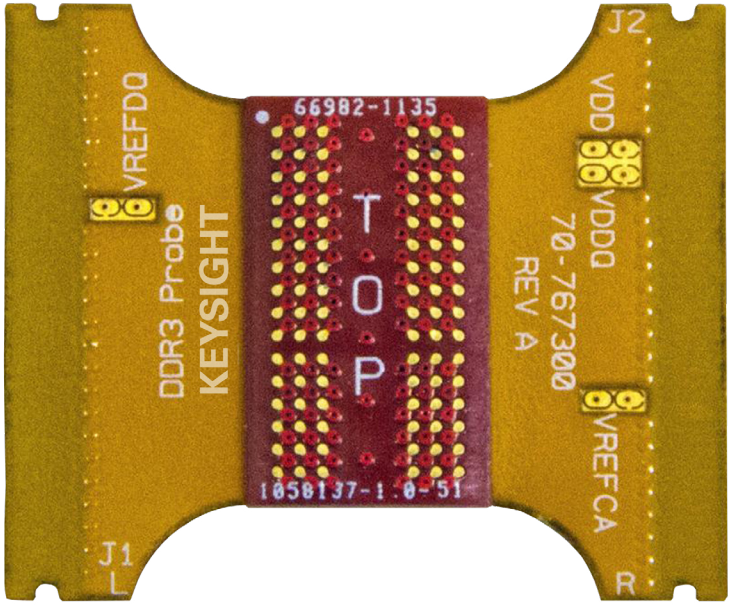
Key features

- Provides connection to (address, command, control, and data) signals between a U4164A logic analysis system and JEDEC- standard 96 ball DDR3 x16 DRAM.
- Provides observation of data traffic on industry-standard 96 ball DDR3 x16 non-stacked DRAMs.
- Provides access for DDR eye scans and burst scans of DDR3 signals.
- Works with all solder finishes and is designed to tolerate lead-free soldering temperature profiles.

The W3636A DDR3 x16 BGA interposer enables you to gain signal access to the DDR3 signals critical to your debug and validation effort through a logic analyzer. The probe works in existing designs and eliminates the need for upfront planning or redesign. The probe connects directly to the balls of the DDR3 x16 non-stacked DRAM or with an optional third-party socket (not provided), enabling the operation and acquisition of high-speed DDR3 signals without impacting the performance of your design.

Specifications

- Standard: DDR3
- Ball count: 96
- DRAM type: x16



Use with oscilloscope requires

- W3635A scope probe adapter(s)
- E2678B socketed probe head(s)
- Oscilloscope probe(s)

Use with logic analyzer requires

- Qty (1) E5845A ZIF probe
- Qty (2) U4201A logic analyzer cables
- Qty (1) U4164A module in AXIe chassis or 16864A logic analyzer
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable, required for U4164A solution
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4 LPDDR2/3/4 and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module with minimum of U4164A-01G speed grade option

W3635A SCOPE PROBE ADAPTER

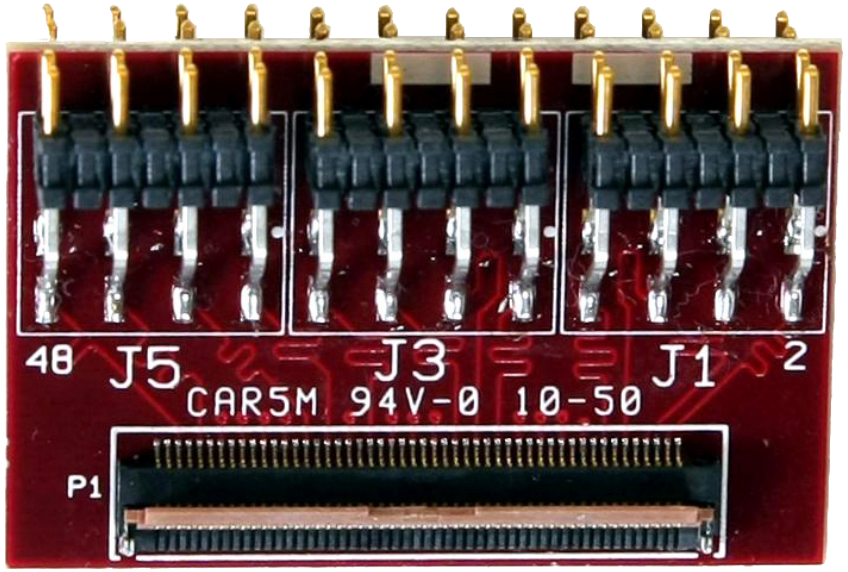
Scope board probe adapter for use with W3630A Series DDR3 BGA probes. The DDR3 BGA probe is used with W3635B scope probe adapter and the E2678A socketed probe head to connect to the oscilloscope. The socketed probe head makes a 4 GHz bandwidth (typical) connection with the pin headers on the W3635B scope probe adapter with N5465A InfiniiSim Waveform Transformation toolset.

Specifications

- Standard: DDR3
- Ball count: 78
- DRAM type: x4x8
- Optimized for oscilloscopes and logic analyzers

Requires

- W3631A, W3633A, or W3636A
- DDR3 BGA interposer
- E2678B socketed probe head(s)
- Oscilloscope probe(s)
- Oscilloscope



E5847A SINGLE-ENDED ZIF PROBE

Key features

- Connects to the W3633A DDR3 BGA probe to enable viewing of industry-standard DDR3 DIMMs with a U4164A or 16864A Series logic analyzer.

A 46-channel single-ended ZIF probe for x8 DRAM BGA probe connection to a 90-pin logic analyzer cable.

Specifications

- Standard: DDR3
- Optimized for logic analyzers

Signal access

- Provides 46 channels: 44 single-ended data, two differential clocks

Probe performance

- 1.5 pF equivalent load capacitance
- 1333 Mb/s maximum data rate
- Measure signals with as little as 250 mV p-p signal amplitude

Connectivity

- Provides a convenient, reliable connection to the W3633A DDR3 DRAM BGA probe

Compatible with

- Logic analyzers with 90-pin cable connectors logic analyzer cable connectors
- The Keysight E5847A ZIF probe connects to the W3633A DDR3 BGA probe to enable viewing of industry-standard DDR3 DRAM with a U4164A or 16864A Series logic analyzer.

Requires

- Qty (1) W3633A BGA interposer
- Qty (1) U4164A module in AXIe chassis or 16864A logic analyzer
- Qty (2) U4201A logic analyzer cables
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable, required for U4164A solution
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4 LPDDR2/3/4 and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module

W2633B DDR2 X8 BGA COMMAND AND DATA PROBE

Key features

- Provides electrically and mechanically nonintrusive connection to all signals between a U4164A or 16864A Series logic analysis system and DDR2 x8 DRAMs.
- Provides access to DDR2 signals in existing designs with no need for redesign or upfront planning. Provides ability to use either leaded or lead-free solder.
- Measurement accuracy and signal integrity insight via DDR Eyefinder and Eyescan software.

The W2633B enables viewing of data traffic on industry-standard DDR2 x8 DRAM with the U4164A and 16864A logic analyzers and X-Series, V-Series, MXR-Series, and UXR-Series oscilloscopes. State speed options for the logic analyzers and bandwidth of the scopes will vary depending on the data rate of the system under test.

Specifications

- JEDEC standard: DDR2
- Ball count: 84-ball
- DRAM type: x8

Use with oscilloscope requires

- W2639A scope probe adapter(s)
- E2678B socketed probe head(s)
- Oscilloscope probe(s)
- Oscilloscope

Use with logic analyzer requires

- Qty (1) E5384A ZIF probe
- Qty (1) U4164A module in AXIe chassis or 16864A logic analyzer
- Qty (2) U4201A logic analyzer cables
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable, required for U4164A solution
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4 LPDDR2/3/4 and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module

W2631B DDR2 X16 BGA COMMAND AND DATA PROBE

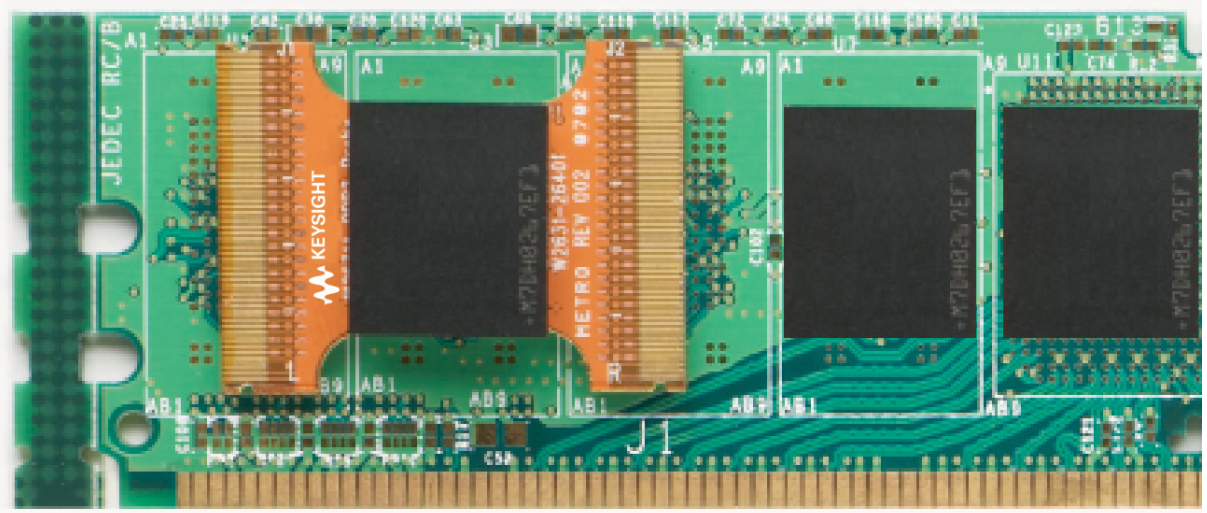
Key features

- Provides electrically and mechanically nonintrusive connection to all signals between a U4164A or 16864A Series logic analysis system and DDR2 x16 DRAMs.
- Access to DDR2 signals in existing designs with no need for re-design or upfront planning. Ability to use either leaded or lead-free solder.
- Measurement accuracy and signal integrity insight via DDR Eyefinder and Eyescan software.

The W2631B enables viewing of data traffic on industry-standard DDR2 DRAM with the U4164A and 16864A logic analyzers and X-Series, V-Series, MXR-Series, and UXR-Series oscilloscopes. State speed options for the logic analyzers and bandwidth of the scopes will vary depending on the data rate of the system under test. The Keysight DDR2 BGA probe for logic analyzer and scope enables viewing of data traffic on industry-standard DDR2 DRAM with the Keysight U4164A.

Specifications

- Standard: DDR2
- Ball count: 92
- DRAM type: x16
- Optimized for oscilloscopes and logic analyzers



Use with Oscilloscope Requires

- W2639A scope probe adapter(s)
- E2678B socketed probe head(s)
- Oscilloscope probe(s)
- Oscilloscope

Use with Logic Analyzer Requires

- Qty (1) E5384A ZIF probe
- Qty (1) U4164A module in AXIe chassis or 16864A logic analyzer
- Qty (2) U4201A logic analyzer cables
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable, required for U4164A solution
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-1TP/-1FP/-1NP DDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4 LPDDR2/3/4 and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module

LPDDR Oscilloscope Interposers

LPDDR5 315 SIGNAL INTEGRITY INTERPOSER

Key features

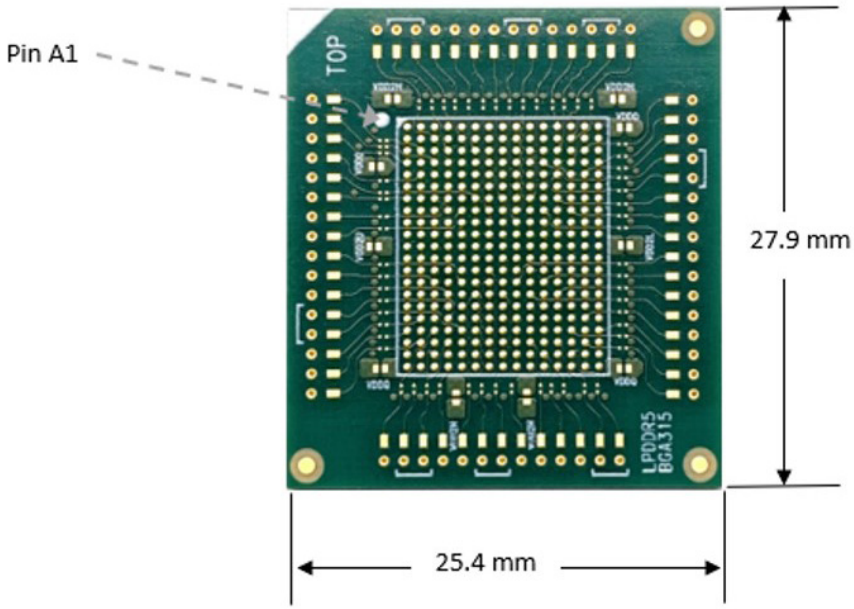
- Probes JEDEC-standard MO-338 LPDDR5 315 Ball, 0.8 mm pitch 15 columns by 0.7 mm 21 rows, 2 channel X 32 DRAM.
- Provides access to selected bus signals between the processor and LPDDR5 memory chip.
- Includes riser for tight KOV applications. The 0.49" X 0.59" riser passes all signals, power, and ground between the processor and memory.
- Interposer and riser thickness are 1.0 mm and 1.7 mm, respectively.

The LPDDR5 315 signal integrity interposer enables probing of embedded LPDDR5-4800 DRAMs and is optimized for use with Keysight's MX0100A InfiniiMax II Micro Pro.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	VDDQ	DMI0_A	GND	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	GND	DMI1_A	VDDQ	NC	NC	A
B	NC	VDDQ	RDQS0t_A	GND	DQ4_A	VDD2L	VDD2H	GND	VDD2H	VDD2L	DQ12_A	GND	RDQS1t_A	VDDQ	NC	B
C	VDD1	DQ1_A	VDDQ	RDQS0c_A	GND	DQ5_A	VDD2H	GND	VDD2H	DQ13_A	GND	RDQS1c_A	VDDQ	DQ9_A	VDD1	C
D	DQ0_A	GND	DQ3_A	VDDQ	WCK0c_A	GND	GND	VDD2H	GND	GND	WCK1c_A	VDDQ	DQ11_A	GND	DQ8_A	D
E	GND	DQ2_A	GND	WCK0t_A	VDDQ	DQ6_A	VDD2H	GND	VDD2H	DQ14_A	VDDQ	WCK1t_A	GND	DQ10_A	GND	E
F	VDDQ	GND	VDDQ	VDDQ	DQ7_A	VDD2H	VDD2H	GND	VDD2H	VDD2H	DQ15_A	VDDQ	VDDQ	GND	VDDQ	F
G	VDDQ	VDDQ	GND	CA0_A	GND	CS1_A	GND	CA2_A	GND	CA4_A	GND	CA6_A	GND	VDDQ	VDDQ	G
H	RESET_n	VDD2L	GND	GND	CA1_A	GND	CS0_A	GND	CKt_A	GND	CA3_A	GND	CA5_A	VDD2L	ZQ_A	H
J	GND	VDD2L	GND	RFU	VDD2H	RFU	GND	GND	CKc_A	GND	VDD2H	GND	GND	VDD2L	GND	J
K	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	GND	GND	GND	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	K
L	GND	GND	GND	GND	GND	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	GND	GND	GND	GND	GND	L
M	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	GND	GND	GND	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	M
N	GND	VDD2L	GND	GND	VDD2H	GND	CKc_B	GND	GND	GND	VDD2H	GND	GND	VDD2L	GND	N
P	RFU	VDD2L	CA5_B	GND	CA3_B	GND	CKt_B	GND	CS0_B	GND	CA1_B	GND	GND	VDD2L	RFU	P
R	VDDQ	VDDQ	GND	CA6_B	GND	CA4_B	GND	CA2_B	GND	CS1_B	GND	CA0_B	GND	VDDQ	VDDQ	R
T	VDDQ	GND	VDDQ	VDDQ	DQ15_B	VDD2H	VDD2H	GND	VDD2H	VDD2H	DQ7_B	VDDQ	VDDQ	GND	VDDQ	T
U	GND	DQ10_B	GND	WCK1t_B	VDDQ	DQ14_B	VDD2H	GND	VDD2H	DQ6_B	VDDQ	WCK0t_B	GND	DQ2_B	GND	U
V	DQ8_B	GND	DQ11_B	VDDQ	WCK1c_B	GND	GND	VDD2H	GND	GND	WCK0c_B	VDDQ	DQ3_B	GND	DQ0_B	V
W	VDD1	DQ_9B	VDDQ	RDQS1c_B	GND	DQ13_B	VDD2H	GND	VDD2H	DQ5_B	GND	RDQS0c_B	VDDQ	DQ1_B	VDD1	W
Y	NC	VDDQ	RDQS1t_B	GND	DQ12_B	VDD2L	VDD2H	GND	VDD2H	VDD2L	DQ4_B	GND	RDQS0t_B	VDDQ	NC	Y
AA	NC	NC	VDDQ	DMI1_B	GND	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	GND	DMI0_B	VDDQ	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

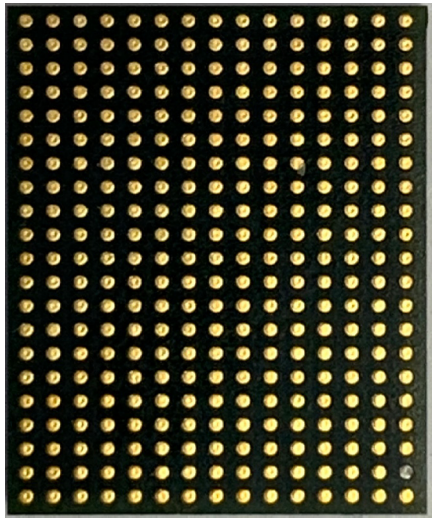
Specifications

- Standard: LPDDR5 Pin Count: 315
- DRAM type: 2 x 32
- DRAM size: 15 mm x 12.4 mm
- Pitch: 0.8 mm x 0.7 mm
- Interposer size: 25.4 mm x 30.5 mm
- JEDEC standard: JEDEC MO-338
- Connectors: Solder-down test points and solder balls on the bottom
- Optimized for use with oscilloscopes



Requires

- X-Series, V-Series, MXR-Series, or UXR-Series oscilloscopes
- Oscilloscope probes with probe heads



LPDDR5 BGA 496 SIGNAL INTEGRITY INTERPOSER

Key features

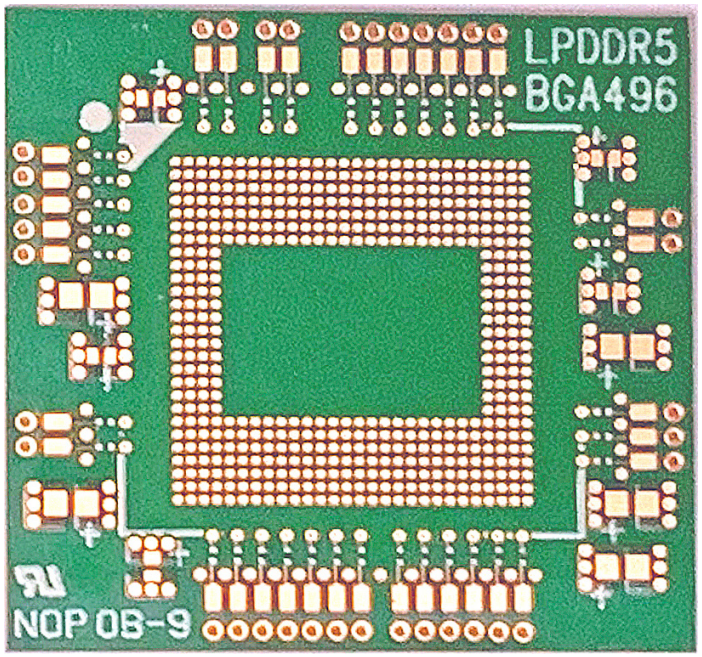
- The LPDDR5 High Performance Signal Integrity Interposer is a rigid, 496 ball, LPDDR5, BGA interposer, optimized for oscilloscope use. This interposer supports the LPDDR5-6400 with Quad x16 Channel LP DRAM memories.
- Probes a 496 ball LPDDR5 Quad x16 Channel LP DRAM chip, JEDEC-standard footprint variation MO-344, with a maximum chip package size of 14 mm X 12.4 mm.
- For tight KOV applications, the DDR5 High Performance Signal Integrity Interposer Kit comes with an LPDDR5 High Performance Riser.
- Interposer and riser thickness are 1.0 mm and 2.0 mm, respectively.

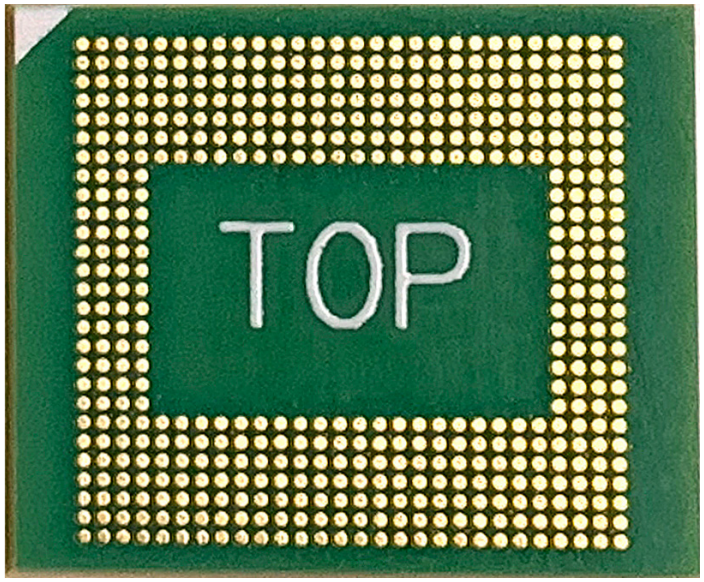
The LPDDR5 High Performance Signal Integrity Interposer is a rigid, 496 ball, LPDDR5, BGA interposer, optimized for use with Keysight's MX0100A InfiniiMax II Micro Probe Head. The interposer goes with the Keysight InfiniiMax I and II probe amplifiers. This interposer supports the LPDDR5-6400 with Quad x16 Channel LP DRAM memories.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
A	NC	NC	VDD1	VDD2H	VDD2L	VDDQ	GND	VDD2H	VDD2L	VDD2H	VDD2H	VDDQ	VDD1	VDD2L	VDD2L	VDD1	VDDQ	VDD2H	VDD2H	GND	VDD2H	VDD2L	VDDQ	VDD2L	VDD2H	VDD1	NC	NC	A
B	NC	DQ3A	RDQS0TA	GND	DQ5A	GND	CS1A	GND	GND	DQ13A	GND	RDQS1TA	GND	DQ9A	DQ1C	GND	RDQS0TC	GND	DQ5C	GND	CS1C	GND	GND	DQ13C	GND	RDQS1TC	DQ11C	NC	B
C	DQ1A	GND	RDQS0CA	DMI0A	VDDQ	CA0A	CS0A	CA4A	CA6A	VDDQ	DMI1A	RDQS1CA	DQ11A	VDDQ	VDDQ	DQ3C	RDQS0CC	DMI0C	VDDQ	CA0C	CS0C	CA4C	CA6C	VDDQ	DMI1C	RDQS1CC	GND	DQ9C	C
D	VDDQ	DQ2A	VDDQ	GND	DQ6A	GND	CA2A	CA3A	GND	DQ14A	GND	VDDQ	GND	DQ8A	DQ0C	GND	VDDQ	GND	DQ6C	GND	CA2C	CA3C	GND	DQ14C	GND	VDDQ	DQ10C	VDDQ	D
E	DQ0A	VDDQ	WCK0CA	DQ4A	VDDQ	CA1A	VDD2H	VDD2L	CA5A	VDDQ	DQ12A	WCK1CA	DQ10A	VDDQ	VDDQ	DQ2C	WCK0CC	DQ4C	VDDQ	CA1C	VDD2H	VDD2L	CA5C	VDDQ	DQ12C	WCK1CC	VDDQ	DQ8C	E
F	GND	GND	WCK0TA	GND	DQ7A	GND	CKTA	CKCA	GND	DQ15A	GND	WCK1TA	GND	ZQAC	RESETn	GND	WCK0TC	GND	DQ7C	GND	CKTC	CKCC	GND	DQ15C	GND	WCK1TC	GND	GND	F
G	VDD2H	VDD1	VDD2L	VDDQ	VDD2H	VDD2L	GND	GND	VDD2H	VDD2L	VDD2H	GND	VDD2L	VDD2H	VDD2H	VDD2L	GND	VDD2H	VDD2H	VDD2L	GND	GND	VDD2H	VDD2L	VDDQ	VDD2L	VDD1	VDD2H	G
H	VDD2H	VDD1	VDD2H	VDD2H																					VDD2H	VDD2H	VDD1	VDD2H	H
J	GND	GND	GND	GND																					GND	GND	GND	GND	J
K	GND	GND	GND	GND																					GND	GND	GND	GND	K
L	GND	GND	GND	GND																					GND	GND	GND	GND	L
M	GND	GND	GND	GND																					GND	GND	GND	GND	M
N	GND	GND	GND	GND																					GND	GND	GND	GND	N
P	GND	GND	GND	GND																					GND	GND	GND	GND	P
R	GND	GND	GND	GND																					GND	GND	GND	GND	R
T	GND	GND	GND	GND																					GND	GND	GND	GND	T
U	GND	GND	GND	GND																					GND	GND	GND	GND	U
V	GND	GND	GND	GND																					GND	GND	GND	GND	V
W	GND	GND	GND	GND																					GND	GND	GND	GND	W
Y	VDD2H	VDD1	VDD2H	VDD2H																					VDD2H	VDD2H	VDD1	VDD2H	Y
AA	VDD2H	VDD1	VDD2L	VDDQ	VDD2H	VDD2L	GND	GND	VDD2H	VDD2L	VDD2H	GND	VDD2L	VDD2H	VDD2H	VDD2L	GND	VDD2H	VDD2H	VDD2L	GND	GND	VDD2H	VDD2L	VDDQ	VDD2L	VDD1	VDD2H	AA
AB	GND	GND	WCK1TB	GND	DQ15B	GND	CKCB	CKTB	GND	DQ7B	GND	WCK0TB	GND	RFU	ZQBD	GND	WCK1TD	GND	DQ15D	GND	CKCD	CKTD	GND	DQ7D	GND	WCK0TD	GND	GND	AB
AC	DQ8B	VDDQ	WCK1CB	DQ12B	VDDQ	CA5B	VDD2L	VDD2H	CA1B	VDDQ	DQ4B	WCK0CB	DQ2B	VDDQ	VDDQ	DQ10D	WCK1CD	DQ12D	VDDQ	CA5D	VDD2L	VDD2H	CA1D	VDDQ	DQ4D	WCK0CD	VDDQ	DQ0D	AC
AD	VDDQ	DQ10B	VDDQ	GND	DQ14B	GND	CA3B	CA2B	GND	DQ6B	GND	VDDQ	GND	DQ0B	DQ8D	GND	VDDQ	GND	DQ14D	GND	CA3D	CA2D	GND	DQ6D	GND	VDDQ	DQ2D	VDDQ	AD
AE	DQ9B	GND	RDQS1CB	DMI1B	VDDQ	CA6B	CA4B	CS0B	CA0B	VDDQ	DMI0B	RDQS0CB	DQ3B	VDDQ	VDDQ	DQ11D	RDQS1CD	DMI1D	VDDQ	CA6D	CA4D	CS0D	CA0D	VDDQ	DMI0D	RDQS0CD	GND	DQ1D	AE
AF	NC	DQ11B	RDQS1TB	GND	DQ13B	GND	GND	CS1B	GND	DQ5B	GND	RDQS0TB	GND	DQ1B	DQ9D	GND	RDQS1TD	GND	DQ13D	GND	GND	CS1D	GND	DQ5D	GND	RDQS0TD	DQ3D	NC	AF
AG	NC	NC	VDD1	VDD2H	VDD2L	VDDQ	VDD2H	GND	VDD2L	VDD2H	VDD2H	VDDQ	VDD1	VDD2L	VSS2L	VDD1	VDDQ	VDD2H	VDD2H	VDD2L	VDD2H	GND	VDDQ	VDD2L	VDD2H	VDD1	NC	NC	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	

Specifications

- Ball count: 496
- Pitch: 0.4 mm X 0.4 mm
- Package size: 20 mm X 14 mm



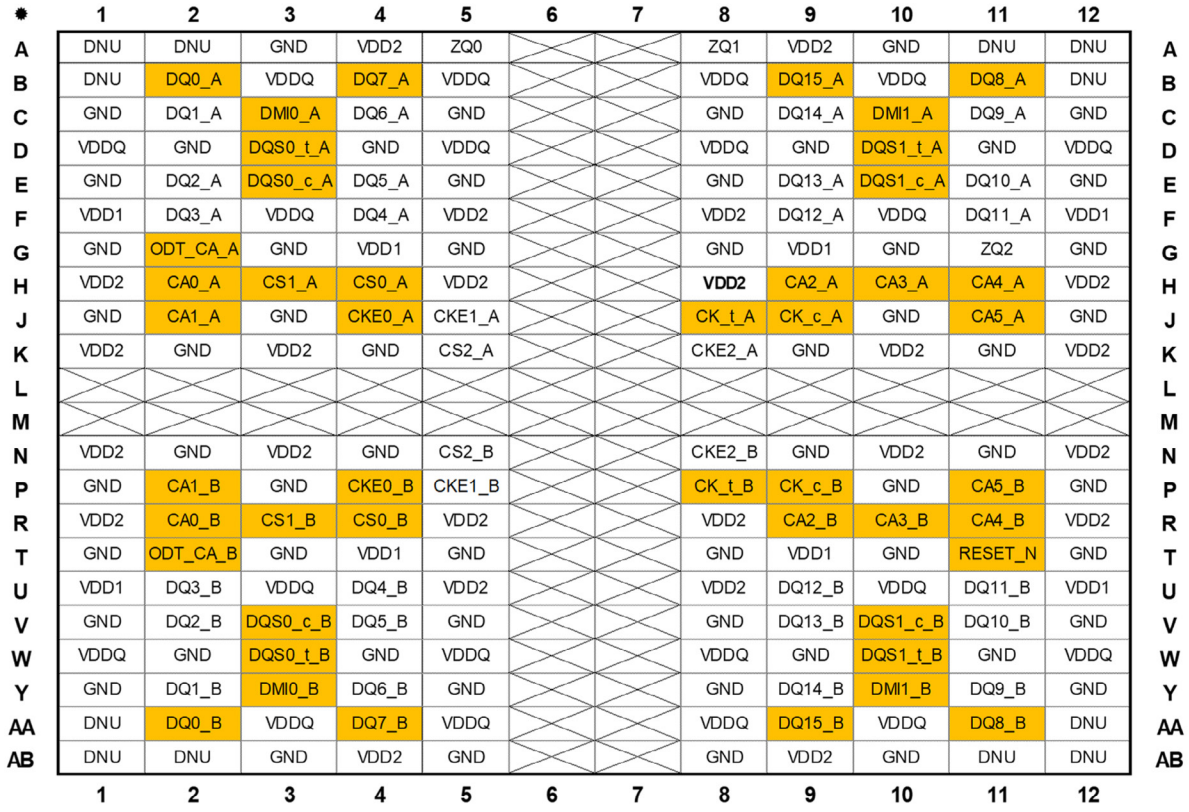


LPDDR4/4X 200 SIGNAL INTEGRITY INTERPOSER

Optimized for oscilloscope measurements, the LPDDR4 200 BGA Signal Integrity Interposer provides access to LPDDR signals and passes all power and ground signals between the processor and the memory chip.

Key features

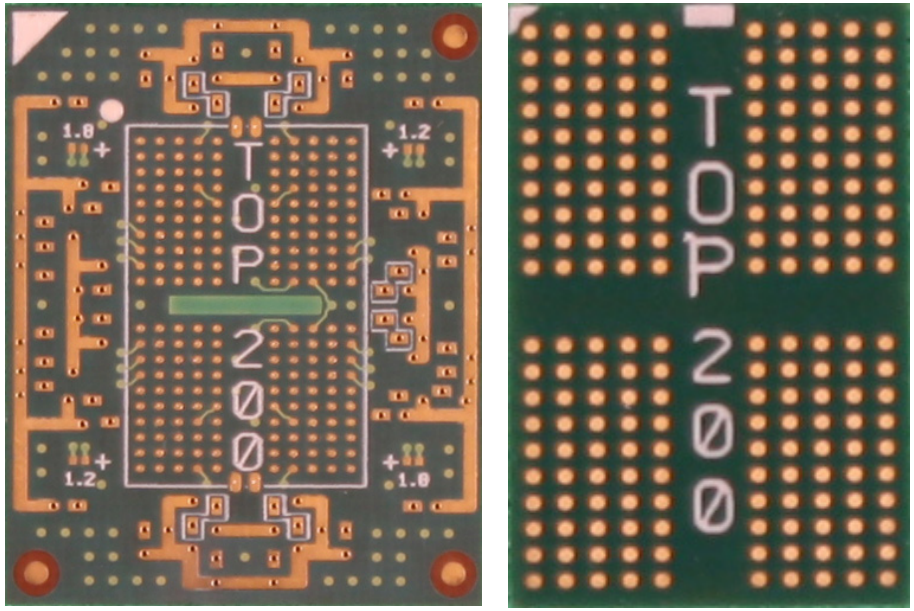
- Enables correct operation of the LPDDR interface while providing access to selected signals between the processor and LPDDR4 memory chip.
- Provides solder-down test pads with plated through-holes that connect to Keysight E2677B or N5381A solder-in probe heads, or N5425A ZIF probe tip.
- Includes S-parameter file to configure the oscilloscope to render waveforms as they exist at the DRAM pins.
- Riser is included to clear surrounding devices in tight keep-out volume applications. Riser dimensions are 10 mm x 15 mm.



✹	1	2	3	4	5	6	7	8	9	10	11	12	
A	DNU	DNU	GND	VDD2	ZQ0			ZQ1	VDD2	GND	DNU	DNU	A
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU	B
C	GND	DQ1_A	DMI0_A	DQ6_A	GND			GND	DQ14_A	DMI1_A	DQ9_A	GND	C
D	VDDQ	GND	DQS0_t_A	GND	VDDQ			VDDQ	GND	DQS1_t_A	GND	VDDQ	D
E	GND	DQ2_A	DQS0_c_A	DQ5_A	GND			GND	DQ13_A	DQS1_c_A	DQ10_A	GND	E
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1	F
G	GND	ODT_CA_A	GND	VDD1	GND			GND	VDD1	GND	ZQ2	GND	G
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2	H
J	GND	CA1_A	GND	CKE0_A	CKE1_A			CK_t_A	CK_c_A	GND	CA5_A	GND	J
K	VDD2	GND	VDD2	GND	CS2_A			CKE2_A	GND	VDD2	GND	VDD2	K
L													L
M													M
N	VDD2	GND	VDD2	GND	CS2_B			CKE2_B	GND	VDD2	GND	VDD2	N
P	GND	CA1_B	GND	CKE0_B	CKE1_B			CK_t_B	CK_c_B	GND	CA5_B	GND	P
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2	R
T	GND	ODT_CA_B	GND	VDD1	GND			GND	VDD1	GND	RESET_N	GND	T
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1	U
V	GND	DQ2_B	DQS0_c_B	DQ5_B	GND			GND	DQ13_B	DQS1_c_B	DQ10_B	GND	V
W	VDDQ	GND	DQS0_t_B	GND	VDDQ			VDDQ	GND	DQS1_t_B	GND	VDDQ	W
Y	GND	DQ1_B	DMI0_B	DQ6_B	GND			GND	DQ14_B	DMI1_B	DQ9_B	GND	Y
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU	AA
AB	DNU	DNU	GND	VDD2	GND			GND	VDD2	GND	DNU	DNU	AB
	1	2	3	4	5	6	7	8	9	10	11	12	

Specifications

- Standard: LPDDR4/4x
- Ball count: 200
- DRAM type: 2 x 16
- DRAM size: 10 mm x 15 mm
- Configuration: Dual channel x16 DRAM
  (JEDEC MO-311 footprint)
- Interposer size: 20 mm x 25 mm
- Pitch: 0.8 mm x 0.65 mm
- Connectors: Solder-down test points and solder balls on the bottom
- JEDEC standard: JESD209-4D
- Optimized for use with oscilloscopes



LPDDR3 178 SIGNAL INTEGRITY INTERPOSER

Optimized for oscilloscope measurements, the LPDDR3 178 BGA Interposer provides access to the LPDDR signals and passes all power and ground signals between the processor and the memory chip.

Key features

- Enables correct operation of the LPDDR interface while providing access to selected bus signals between the processor and LPDDR memory chip.
- Provides solder pads for use with the Keysight E2677A or N5381B InfiniiMax single-ended / differential solder-in or Keysight N5425B ZIF probe head.
- Includes an S-parameter file to configure the oscilloscope to render waveforms as they exist at the DRAM pins.
- Includes a 11.5 mm x 11 mm riser to clear surrounding devices in tight KOV applications.

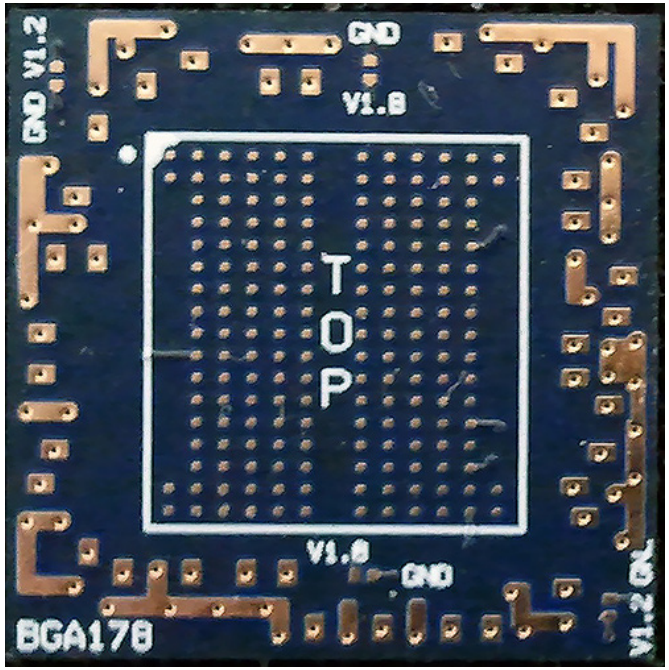
✹	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	A
B	DNU	GND	ZQ0	ZQ1	GND	GND		DQ31	DQ30	DQ29	DQ28	GND	DNU	B
C		CA9	GND	NC	GND	GND		DQ27	DQ26	DQ25	DQ24	VDDQ		C
D		CA8	GND	VDD2	VDD2	VDD2		DM3	DQ15	DQS3_t	DQS3_c	GND		D
E		CA7	CA6	GND	GND	GND		VDDQ	DQ14	DQ13	DQ12	VDDQ		E
F		VDDCA	CA5	GND	GND	GND		DQ11	DQ10	DQ9	DQ8	GND		F
G		VDDCA	GND	GND	VDD2	GND		DM1	GND	DQS1_t	DQS1_c	VDDQ		G
H		GND	VDDCA	VrefCA	VDD2	VDD2		VDDQ	VDDQ	GND	VDDQ	VDD2		H
J		CK_c	CK_t	GND	VDD2	VDD2		ODT	VDDQ	VDDQ	VrefDQ	GND		J
K		GND	CKE0	CKE1	VDD2	VDD2		VDDQ	NC	GND	VDDQ	VDD2		K
L		VDDCA	CS0_n	CS1_n	VDD2	GND		DM0	GND	DQS0_t	DQS0_c	VDDQ		L
M		VDDCA	CA4	GND	GND	GND		DQ4	DQ5	DQ6	DQ7	GND		M
N		CA2	CA3	GND	GND	GND		VDDQ	DQ1	DQ2	DQ3	VDDQ		N
P		CA1	GND	VDD2	VDD2	VDD2		DM2	DQ0	DQS2_t	DQS2_c	GND		P
R		CA0	NC	GND	GND	GND		DQ20	DQ21	DQ22	DQ23	VDDQ		R
T	DNU	GND	GND	GND	GND	GND		DQ16	DQ17	DQ18	DQ19	GND	DNU	T
U	DNU	DNU	VDD1	VDD1	VDD1	VDD1		VDD2	VDD2	VDD1	VDDQ	DNU	DNU	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Specifications

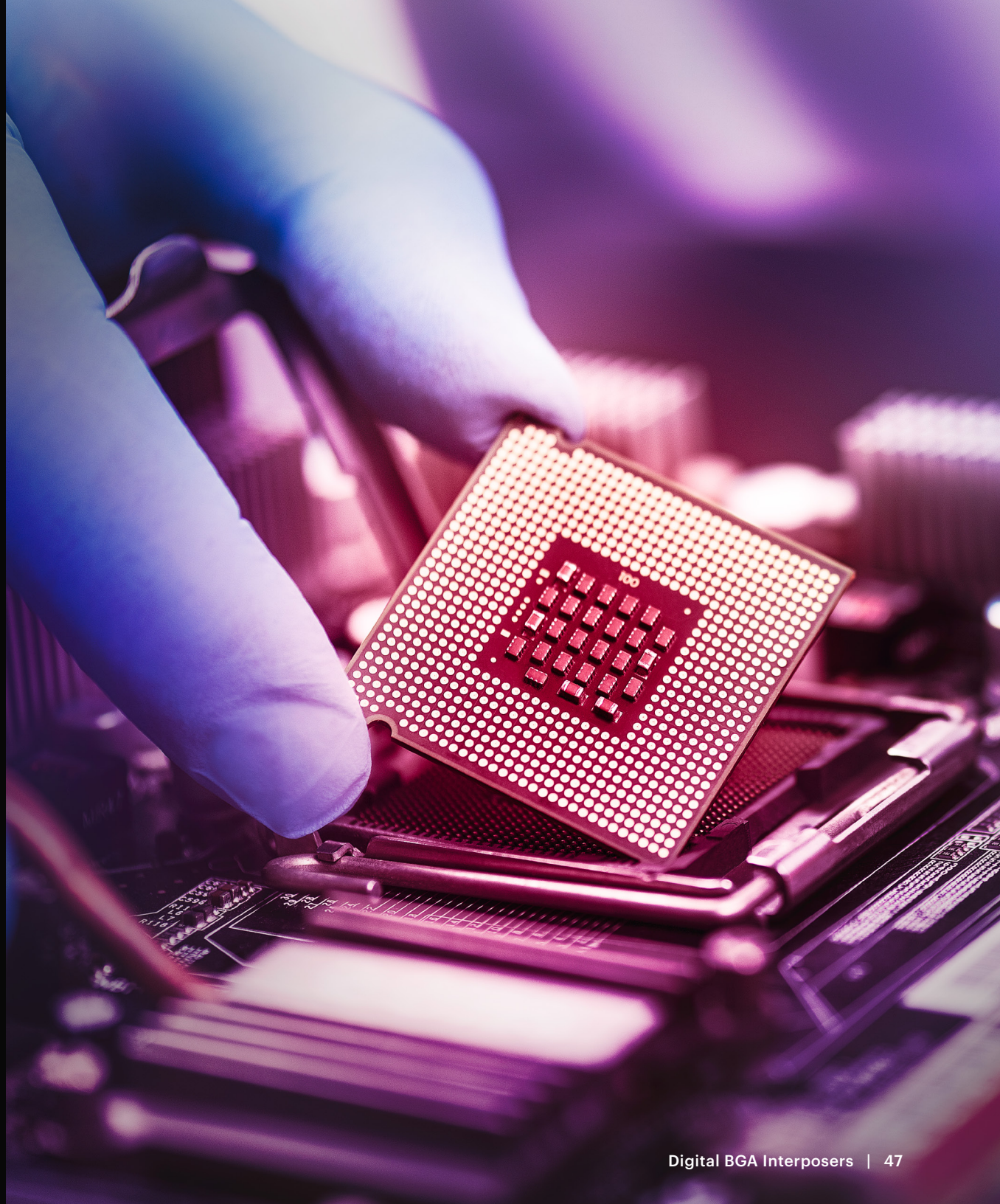
- Standard: LPDDR3
- Ball count: 178
- DRAM type: x32
- DRAM size: 11.5 mm x 11 mm
- Configuration: Single-channel x32 DRAM (JEDEC MO-311A footprint)
- Interposer size: 19 mm x 19 mm
- Pitch: 0.8 mm x 0.65 mm
- Connectors: Solder-down test points and solder balls
- JEDEC standard: JESD209-3B
- Optimized for use with oscilloscopes

Requires

- X-Series, V-Series, MXR-Series, or UXR-Series oscilloscopes
- Oscilloscope probes with probe heads



LPDDR Logic Analyzer Interposers



LPDDR5/5X 315 LOGIC ANALYZER INTERPOSER

The LPDDR5 BGA 315 Logic Analyzer Interposer probes command / address (CA), chip select (CS), Clocks, and Reset pins to provide signal visibility with a logic analyzer solution. All other signals, power, and grounds are passed through between the processor and the memory chip.

Key features

- Probes JEDEC standard MO-338 LPDDR5 315 Ball, 0.8 mm pitch 15 columns by 0.7 mm 21 rows, 2 channel X 32 DRAM.
- Provides access to selected bus signals between the processor and LPDDR5/5x memory chip.
- Enables correct operation of the LPDDR5/5x interface while being probed with Keysight's U4164A logic analyzers for 9600 MT/s+ data rates.
- Provides interface to the U4164A logic analyzer via two U4209A probe cables (not included).
- Includes 0.49" X 0.59" riser for tight KOV applications. The riser passes all signals, power, and ground between the processor and memory.
- Interposer and riser thicknesses are 0.5 mm and 1.7 mm, respectively.

	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	NC	NC	VDD1	DQ8_B	GND	VDDQ	VDDQ	RFU	GND	VDD2H	GND	VDD2H	GND	RESET_n	VDDQ	VDDQ	GND	DQ0_A	VDD1	NC	NC	1
2	NC	VDDQ	DQ_9B	GND	DQ10_B	GND	VDDQ	VDD2L	VDD2L	VDD2H	GND	VDD2H	VDD2L	VDD2L	VDDQ	GND	DQ2_A	GND	DQ1_A	VDDQ	NC	2
3	VDDQ	RDQS1t_B	VDDQ	DQ11_B	GND	VDDQ	GND	CA5_B	GND	VDD2H	GND	VDD2H	GND	GND	GND	VDDQ	GND	DQ3_A	VDDQ	RDQS0t_A	VDDQ	3
4	DMI1_B	GND	RDQS1c_B	VDDQ	WCK1t_B	VDDQ	CA6_B	GND	GND	VDD2H	GND	VDD2H	RFU	GND	CA0_A	VDDQ	WCK0t_A	VDDQ	RDQS0c_A	GND	DMI0_A	4
5	GND	DQ12_B	GND	WCK1c_B	VDDQ	DQ15_B	GND	CA3_B	VDD2H	VDD2H	GND	VDD2H	VDD2H	CA1_A	GND	DQ7_A	VDDQ	WCK0c_A	GND	DQ4_A	GND	5
6	VDD2L	VDD2L	DQ13_B	GND	DQ14_B	VDD2H	CA4_B	GND	GND	VDD2H	VDD2H	VDD2H	RFU	GND	CS1_A	VDD2H	DQ6_A	GND	DQ5_A	VDD2L	VDD2L	6
7	VDD2H	VDD2H	VDD2H	GND	VDD2H	VDD2H	GND	CKt_B	CKe_B	GND	VDD2H	GND	GND	CS0_A	GND	VDD2H	VDD2H	GND	VDD2H	VDD2H	VDD2H	7
8	VDD2H	GND	GND	VDD2H	GND	GND	CA2_B	GND	GND	GND	VDD2H	GND	GND	GND	CA2_A	GND	GND	VDD2H	GND	GND	VDD2H	8
9	VDD2H	VDD2H	VDD2H	GND	VDD2H	VDD2H	GND	CS0_B	GND	GND	VDD2H	GND	CKc_A	CKt_A	GND	VDD2H	VDD2H	GND	VDD2H	VDD2H	VDD2H	9
10	VDD2L	VDD2L	DQ5_B	GND	DQ6_B	VDD2H	CS1_B	GND	GND	VDD2H	VDD2H	VDD2H	GND	GND	CA4_A	VDD2H	DQ14_A	GND	DQ13_A	VDD2L	VDD2L	10
11	GND	DQ4_B	GND	WCK0c_B	VDDQ	DQ7_B	GND	CA1_B	VDD2H	VDD2H	GND	VDD2H	VDD2H	CA3_A	GND	DQ15_A	VDDQ	WCK1c_A	GND	DQ12_A	GND	11
12	DMI10_B	GND	RDQS0c_B	VDDQ	WCK0t_B	VDDQ	CA0_B	GND	GND	VDD2H	GND	VDD2H	GND	GND	CA6_A	VDDQ	WCK1t_A	VDDQ	RDQS1c_A	GND	DMI1_A	12
13	VDDQ	RDQS0t_B	VDDQ	DQ3_B	GND	VDDQ	GND	GND	GND	VDD2H	GND	VDD2H	GND	CA5_A	GND	VDDQ	GND	DQ11_A	VDDQ	RDQS1t_A	VDDQ	13
14	NC	VDDQ	DQ1_B	GND	DQ2_B	GND	VDDQ	VDD2L	VDD2L	VDD2H	GND	VDD2H	VDD2L	VDD2L	VDDQ	GND	DQ10_A	GND	DQ9_A	VDDQ	NC	14
15	NC	NC	VDD1	DQ0_B	GND	VDDQ	VDDQ	RFU	GND	VDD2H	GND	VDD2H	GND	ZQ_A	VDDQ	VDDQ	GND	DQ8_A	VDD1	NC	NC	15
	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Specifications

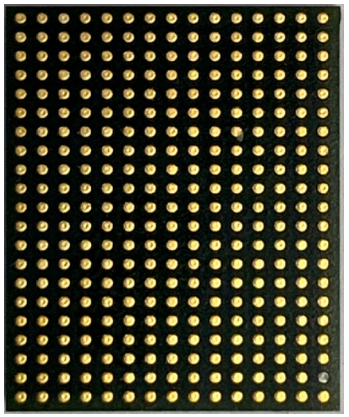
- Standard: LPDDR5/5x
- Pin count: 315
- DRAM type: 2x32
- DRAM size: 15 mm x 12.4 mm
- Interposer size: 18.8 mm X 21.6 mm
- Pitch: 0.8 mm x 0.7 mm
- JEDEC standard: JESD209-5B

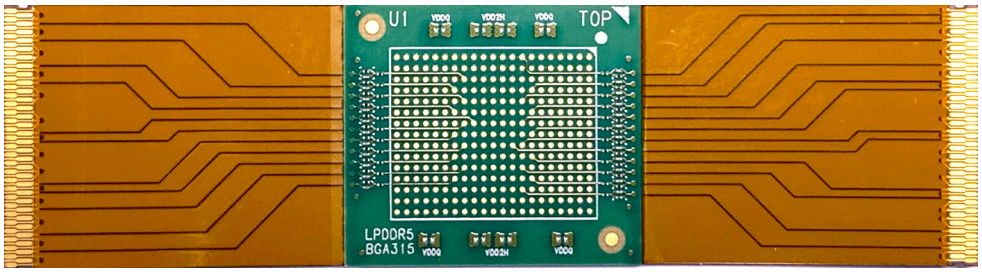
Requires

- Qty (2) U4164A module in AXIe chassis with minimum of U4164A-01G speed option.
- Qty (2) U4209A probe cables
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable required for U4164A solution
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-6TP/-6FP/-6NP LPDDR5 Analysis and Compliance Validation
- Memory depth option of choice for U4164A logic analyzer module





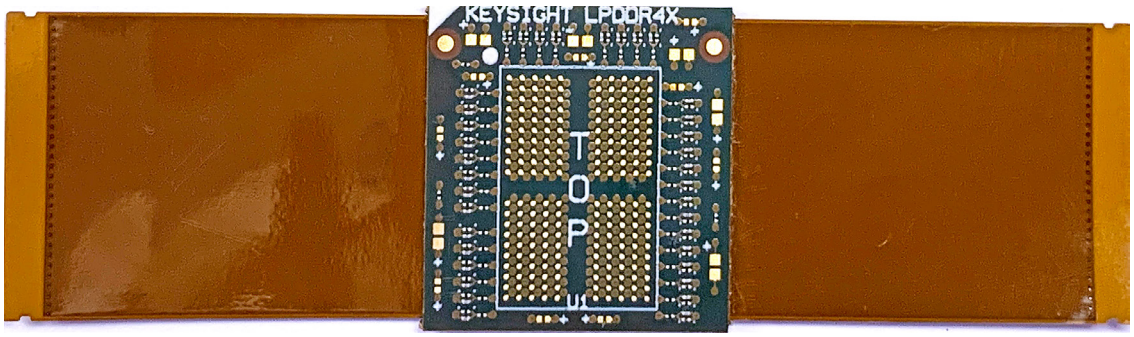
LPDDR4/4X 200 LOGIC ANALYZER INTERPOSER

Key features

- Provides connection to all channel A Bank 0 and Bank 1, address, command, and control between a U4164A logic analysis system and JEDEC standard 200-ball LPDDR4/4x DRAM.
- Provides observation of partial data traffic on industry-standard, 200-ball LPDDR4/4x DRAM, and provides access for DDR eye scans and burst scans of LPDDR4/4x signals.
- Ships with a custom 200-ball LPDDR4/4x riser to reduce KOV under the interpose. The riser can be replaced with an optional third-party socket that is not included; it works with all solder finishes and is designed to tolerate lead-free soldering temperature profiles.

The LPDDR4/4x two-wing BGA interposer for LPDDR4/4x 200-ball BGA DRAM probing takes full advantage of the quad sample state mode on the U4164A logic analyzer module it is compatible with. The W6601A is the smallest BGA interposer for the LPDDR4/4x 200-ball DRAM, capable of capturing simultaneous read and write traffic at data rates more than 3.2 Gb/s. The U4208A and U4209A probe / cables connect the W6601A LPDDR4/4x BGA interposer directly to the U4164A logic analyzer module from 61-pin high-density zero insertion force (ZIF) connectors that attach to the W6601A BGA interposer wings. Refer to the W6601A data sheet for a complete list of LPDDR4 signals the W6601A probes.

The LPDDR4/4x 200-ball BGA interposer enables signal access to the LPDDR4/4x signals critical to your debug and validation effort through a U4164A logic analyzer. The probe works in existing designs and eliminates the need for upfront planning or redesign. The probe connects directly to the balls of the DRAM using an LPDDR4/4x 200-ball riser (included) or an optional third-party socket (not included), enabling the operation and acquisition of high-speed LPDDR4 signals.



Specifications

- Standard: LPDDR4/4x ball count: 200
- DRAM type: Dual x 16 channels DRAM
- Size: 10 mm x 15 mm
- Pitch: 0.8 mm x 0.65 mm
- JEDEC standard: JEDEC
- MO-311 footprint
- Optimized for use with logic analyzers

Requires

- Qty (2) U4164A logic analyzer module with option -02G for quad sample state mode
- Chassis for U4164A logic analyzer module(s) with controller or host PC
- Qty (1) U4208A probe / cable, 61-pin ZIF, no RC, 160-pin direct connect
- Qty (1) U4209A probe / cable, 61-pin ZIF, no RC,160-pin direct connect
- B4661A Memory Analysis software (base software for DDR Setup Assistant and default configurations)

Recommended

- B4661A Memory Analysis software and licensed options:
  - B4661A-2TP/-2FP/-2NP LDDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for the U4164A logic analyzer

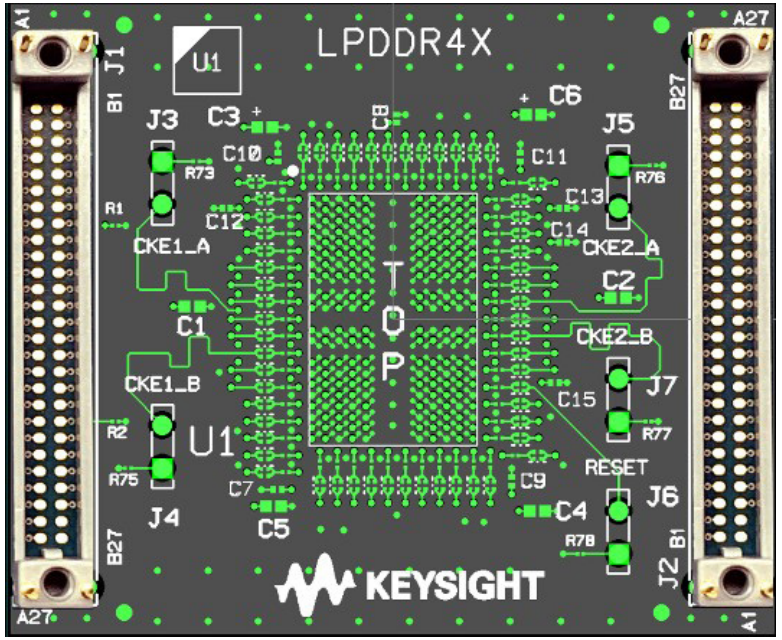
LPDDR4/4X 200 RIGID LOGIC ANALYZER INTERPOSER

Key features

- A LPDDR4/4x 200-ball rigid BGA interposer tested to 4266MT/s. CA/CNTRL capture accurate to 4266MT/s. DQ capture accurate to 3200MT/s
- Provides connection to all address, command, control, DQS, and DQ from an LPDDR4/4x 200-ball package to two U4164A logic analyzer modules using two U4207A RC zero ohm, SoftTouchPro direct connect probes
- Passively probes LPDDR4/4x 200-ball package

The LPDDR4/4x rigid RC BGA interposer for the LPDDR4/4x 200-ball DRAM enables the capture of simultaneous read and write traffic at data rates and has been tested to 4266 MT/s. Two U4207A zero Ω, 34-channel, soft touch pro, single-ended, 4 x 160-pin direct connect probes are required to connect the LPDDR4/4x BGA interposer into two U4164A logic analyzer modules.

The LPDDR4/4x rigid RC BGA interposer enables signal access to the LPDDR4/4x signals critical to your debug and validation effort through a U4164A logic analyzer system. The probe works in existing designs and eliminates the need for upfront planning or redesign. The probe connects directly to the balls of the DRAM using an LPDDR4/4x 200-ball riser (included) or an optional third-party socket (not provided), enabling the operation and acquisition of LPDDR4/4x signals.



Specifications

- Standard: LPDDR4/4x
- Pin count: 200
- DRAM type: Dual x16 channels
- DRAM size: 10 mm x 15 mm
- Pitch: 0.8 mm x 0.65 mm
- JEDEC standard: JEDEC (MO-311 footprint)
- Optimized for use with logic analyzers

Requires

- Qty (2) U4164A logic analyzer module, each with option -02G for quad sample state mode
- Chassis for U4164A logic analyzer module(s) with controller or host PC
- Qty (2) U4207A probe / cable, Soft touch Pro to 160-pin direct connect
- B4661A Memory Analysis software (base software for DDR Setup Assistant and default configurations)

Recommended

- B4661A Memory Analysis software and licensed options:
  - B4661A-2TP/-2FP/-2NP LDDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for the U4164A logic analyzer

LPDDR4 200 LOGIC ANALYZER INTERPOSER

The LPDDR4 200-ball single-wing BGA logic analyzer interposer is optimized for protocol measurements with a Keysight logic analyzer. It provides access to the highlighted LPDDR signals and passes all power and ground signals between the processor and the memory chip.

Key features

- Enables correct operation of the LPDDR interface while providing access to selected signals between the processor and LPDDR4 memory chip. Probes a single clock to support a single data channel operation.
- Rigid-flex-rigid structure with one soft touch Pro connector. Requires one modified E5406A cable (sold separately) to connect to the logic analyzer.
- Includes configuration file for set up of the logic analyzer.
- Includes a 10 x 15 mm riser to clear surrounding devices in tight KOV applications.
- This interposer is only for LPDDR4, it does NOT cover LPDDR4x

✹	1	2	3	4	5	6	7	8	9	10	11	12	
A	DNU	DNU	GND	VDD2	ZQ0			ZQ1	VDD2	GND	DNU	DNU	A
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU	B
C	GND	DQ1_A	DMI0_A	DQ6_A	GND			GND	DQ14_A	DMI1_A	DQ9_A	GND	C
D	VDDQ	GND	DQS0_t_A	GND	VDDQ			VDDQ	GND	DQS1_t_A	GND	VDDQ	D
E	GND	DQ2_A	DQS0_c_A	DQ5_A	GND			GND	DQ13_A	DQS1_c_A	DQ10_A	GND	E
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1	F
G	GND	ODT_CA_A	GND	VDD1	GND			GND	VDD1	GND	ZQ2	GND	G
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2	H
J	GND	CA1_A	GND	CKE0_A	CKE1_A			CK_t_A	CK_c_A	GND	CA5_A	GND	J
K	VDD2	GND	VDD2	GND	CS2_A			CKE2_A	GND	VDD2	GND	VDD2	K
L													L
M													M
N	VDD2	GND	VDD2	GND	CS2_B			CKE2_B	GND	VDD2	GND	VDD2	N
P	GND	CA1_B	GND	CKE0_B	CKE1_B			CK_t_B	CK_c_B	GND	CA5_B	GND	P
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2	R
T	GND	ODT_CA_B	GND	VDD1	GND			GND	VDD1	GND	RESET_N	GND	T
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1	U
V	GND	DQ2_B	DQS0_c_B	DQ5_B	GND			GND	DQ13_b	DQS1_c_B	DQ10_B	GND	V
W	VDDQ	GND	DQS0_t_B	GND	VDDQ			VDDQ	GND	DQS1_t_B	GND	VDDQ	W
Y	GND	DQ1_B	DMI0_B	DQ6_B	GND			GND	DQ14_B	DMI1_B	DQ9_B	GND	Y
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU	AA
AB	DNU	DNU	GND	VDD2	GND			GND	VDD2	GND	DNU	DNU	AB
	1	2	3	4	5	6	7	8	9	10	11	12	

Specifications

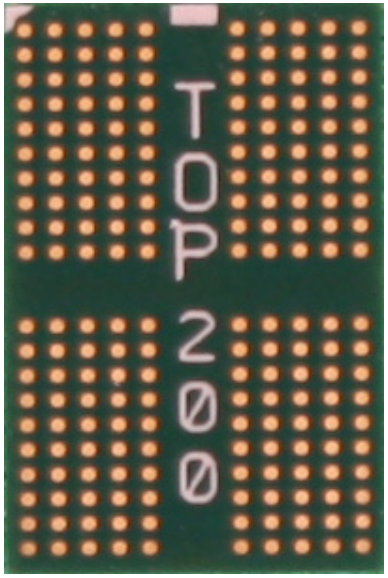
- Standard: LPDDR4
- Ball count: 200
- DRAM type: x32
- DRAM size: 10 x 15 mm
- Configuration: Single channel x32 DRAM (JEDEC MO-311 footprint)
- Interposer size (rigid portion): 19 mm x 21 mm
- Pitch: 0.8 mm x 0.65 mm
- Optimized for use with logic analyzers

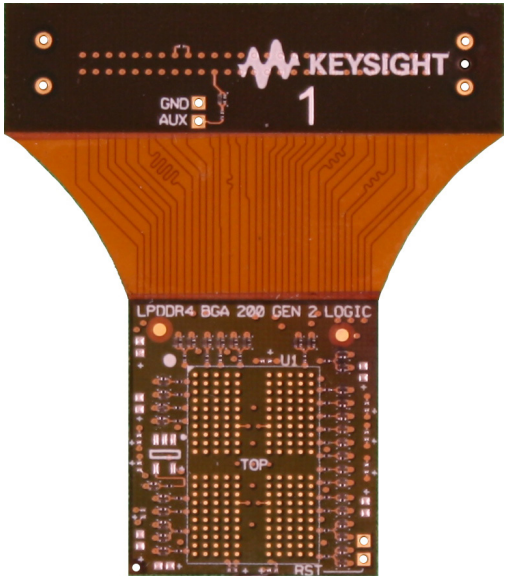
Requires

- Qty (1) modified E5406A probe
- Qty (1) U4164A module in AXIe chassis
- Qty (2) U4201A logic analyzer cables
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software and licensed options:
  - B4661A-2TP/-2FP/-2NP LDDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module with minimum of U4164A-01G speed grade option





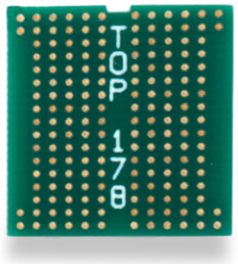
W3301A LPDDR3 178-BALL BGA INTERPOSER

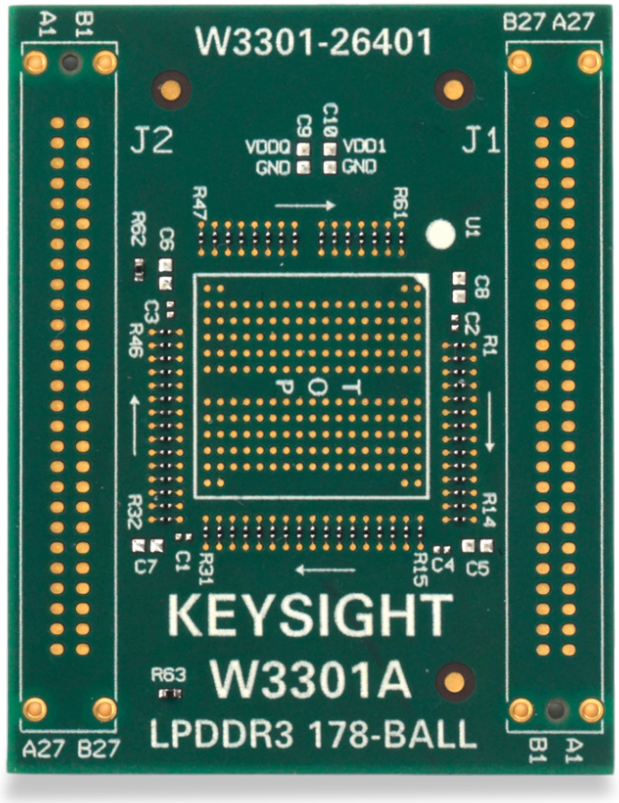
Key features

- The LPDDR3 178-ball BGA interposer is designed to achieve up to 1866 Mb/s data rates. Provides connection to all address, command, control, DQSt, and DQ between a U4164A logic analysis system and JEDEC-standard 178-ball LPDDR3 DRAM.
- Provides access for DDR eye scans and burst scans of LPDDR3 signals.
- The W3301A ships with a custom 178-ball LPDDR3 riser to reduce KOV under the interposer. The riser can be replaced with an optional third-party socket (not provided).
- Works with all solder finishes and tolerates lead-free soldering temperature profiles.

The W3301A LPDDR3 rigid BGA interposer for LPDDR3 178-ball DRAM enables the capture of simultaneous read and write traffic at data rates up to 1866 Mb/s. E5406A Soft Touch probes and U4201A cables connect the W3301A LPDDR3 BGA interposer to the U4164A logic analyzer module.

The W3301A LPDDR3 178-ball rigid BGA interposer enables signal access to the LPDDR3 signals critical to your debug and validation effort through a U4164A logic analyzer. The probe works in existing designs and eliminates the need for upfront planning or redesign. The probe connects directly to the balls of the DRAM using an LPDDR3 178-ball riser (included) or an optional third-party socket (not provided), enabling the operation and acquisition of LPDDR3 signals.





Specifications

- Standard: LPDDR3
- Ball count: 178
- DRAM size: 13.5 x 13 mm
- Optimized for use with logic analyzers

Requires

- Qty (2) E5406A Soft touch Pro probes
- Qty (4) U4201A logic analyzer cables
- Qty (1) U4164A module in AXIe chassis or 16864A logic analyzer
- M9537A embedded controller or host PC with PCIe® adapter card and PCIe® x8 cable
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software and licensed options:
  - B4661A-2TP/-2FP/-2NP LDDR2/3/4 Listing Decoder
  - B4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module with minimum of U4164A-01G speed grade option

W2637A LPDDR BGA PROBES

Key features

- Provides signal accessibility points for the LPDDR SDRAM, LPDDR NVM, and mobile-DDR DRAM BGA package.
- Offers operating transfer rate of up to 400 Mb/s, 1.5 GHz bandwidth.
- Provides signal isolation and minimizes capacitive loading with buried resistors.
- Attaches to W2639A LPDDR scope adapter board and E2678A for connection to the oscilloscope.
- Attaches with the E5384A, single-ended ZIF probe for connection to the logic analyzer.

The W2637A LPDDR BGA probe allows you to get complete signal access to the LPDDR and mobile-DDR signals critical to your debug and validation effort with Keysight logic analyzers and oscilloscopes. The LPDDR BGA probes enable viewing of data traffic on industry standards LPDDR SDRAM, LPDDR NVM and mobile-DDR SDRAM. The probe works in existing designs and eliminates the need for up front planning or re-design. The probe connects directly to the balls of the DRAM, enabling you to operate at full speed and acquire high-speed LPDDR signals without impacting the performance of your design.

Specifications

- Standard: LPDDR
- Ball Count: 60
- DRAM Type: x16
- Optimized for Oscilloscopes and Logic Analyzers

Use with oscilloscope requires

- W2639A scope adapter
- X-Series, V-Series, MXR-Series, or UXR-Series oscilloscopes
- Oscilloscope probes with probe heads

Use with logic analyzer requires

- E5384A ZIF probe
- U4164A module in AXIe chassis or 16864A logic analyzer
- Qty (2) U4201A logic analyzer cables
- M9537A embedded controller or host PC with PCI®e adapter card and PCI®e x8 cable, required for U4164A solution
- B4661A Memory Analysis software

Recommended

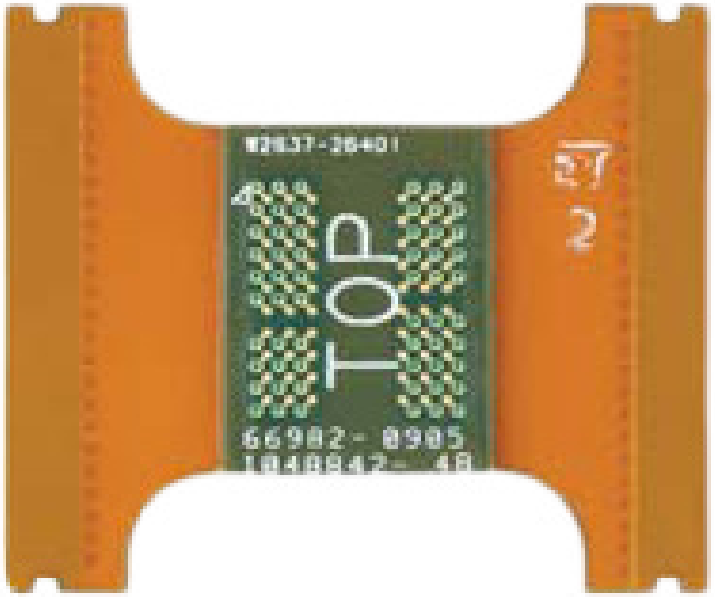
- B4661A Memory Analysis software licensed options:
  - B4661A-2TP/-2FP/-2NP DDR2/3/4 Listing Decoder
  - 4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module

W2638A LPDDR BGA PROBES

Key features

- Provides signal accessibility points for the LPDDR SDRAM, LPDDR NVM, and mobile-DDR DRAM BGA package.
- Operates transfer rate of up to 400 Mb/s, 1.5 GHz bandwidth
- Buried resistors provide signal isolation and minimize capacitive loading.
- Attach to W2639A LPDDR scope adapter board and E2678A for connection to the oscilloscope.
- Attach to E5384A single-ended ZIF probe for connection to the logic analyzer.

The W2638A LPDDR BGA probe enables you to get complete signal access to the LPDDR and mobile DDR signals critical to your debug and validation effort with Keysight logic analyzers and oscilloscopes. The LPDDR BGA probes enable viewing of data traffic on industry standards LPDDR SDRAM, LPDDR NVM, and mobile-DDR SDRAM. The probe works in existing designs and eliminates the need for up front planning or redesign. It connects directly to the balls of the DRAM, enabling you to operate at full speed and acquire high-speed LPDDR signals without impacting the performance of your design.



Specifications

- Standard: LPDDR2/3/4
- Ball count: 90
- DRAM Type: x32

Use with oscilloscope requires

- W2639A scope adapter
- X-Series, V-Series, MXR-Series, or UXR-Series oscilloscopes
- Oscilloscope probes with probe heads

Use with logic analyzer requires

- E5384A ZIF probe
- U4164A module in AXIe chassis or 16864A logic analyzer
- Qty (2) U4201A logic analyzer cables
- M9537A embedded controller or host PC with PCI®e adapter card and PCI®e x8 cable, required for U4164A solution
- B4661A Memory Analysis software

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-2TP/-2FP/-2NP DDR2/3/4 Listing Decoder
  - 4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module

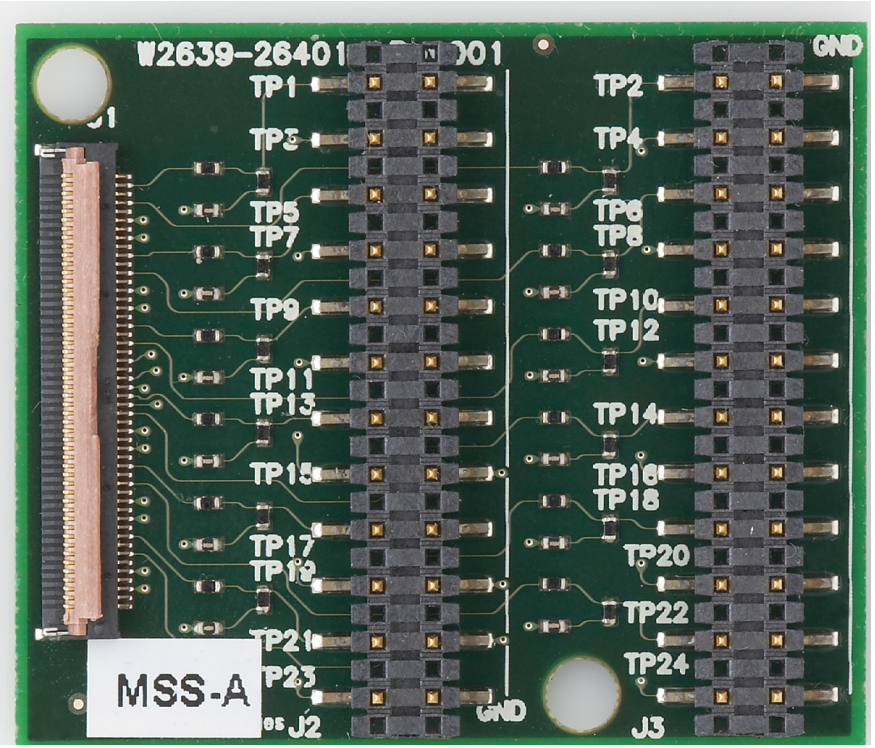
W2639A LPDDR GBA PROBE

Attaching the W2639A scope adapter to the W2637A or W2638A LPDDR BGA probes enables you to get complete signal access to the LPDDR and mobile -DDR signals critical to your debug and validation effort with Keysight logic analyzers and oscilloscopes. The LPDDR BGA probes enable viewing of data traffic on industry standards LPDDR SDRAM, LPDDR NVM, and mobile-DDR SDRAM. The probe works in existing designs and eliminates the need for upfront planning or re-design. The probe connects directly to the balls of the DRAM, enabling you to operate at full speed and acquire high-speed LPDDR signals without impacting the performance of your design.

Use the LPDDR BGA probe with the W2639A scope adapter board and the E2678A scope socket probe head to connect to the oscilloscope. The scope socket probe head attaches to the pin headers on the scope adapter board. The scope socket probe head makes a 1.5 GHz bandwidth connection with the solder points on the BGA probe.

Specifications

- Standard: LPDDR



LPDDR2 121 LOGIC ANALYZER INTERPOSER

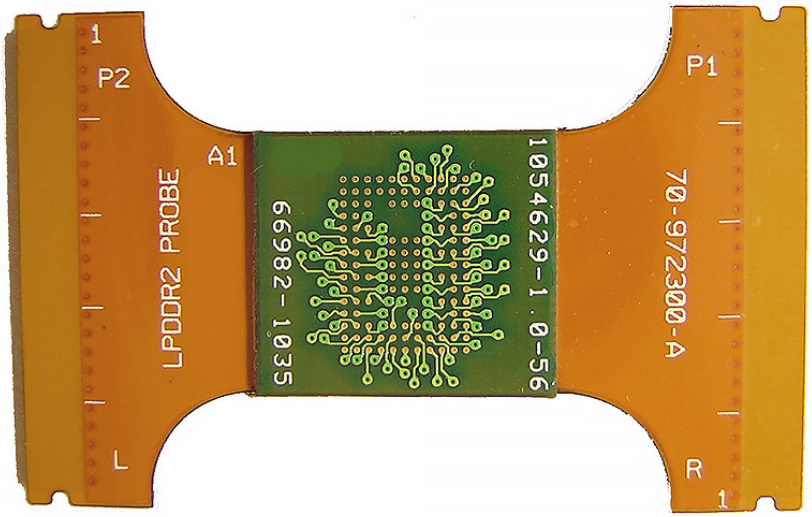
Key features

- Enables correct operation of the LPDDR 2 interface while providing access to selected bus signals between the processor and LPDDR2 memory chip.
- Rigid / flex probe can be soldered in place or used with a BGA socket.

Optimized for logic analyzer measurements, the LPDDR2 121-ball BGA interposer can also be used for oscilloscope measurements. The interposer provides access to the LPDDR signals passes all power and ground signals between the processor and the memory chip.

Specifications

- Standard: LPDDR2
- Ball count: 121
- DRAM type: x16
- DRAM size: 10 mm x 11 mm



Use with oscilloscope requires

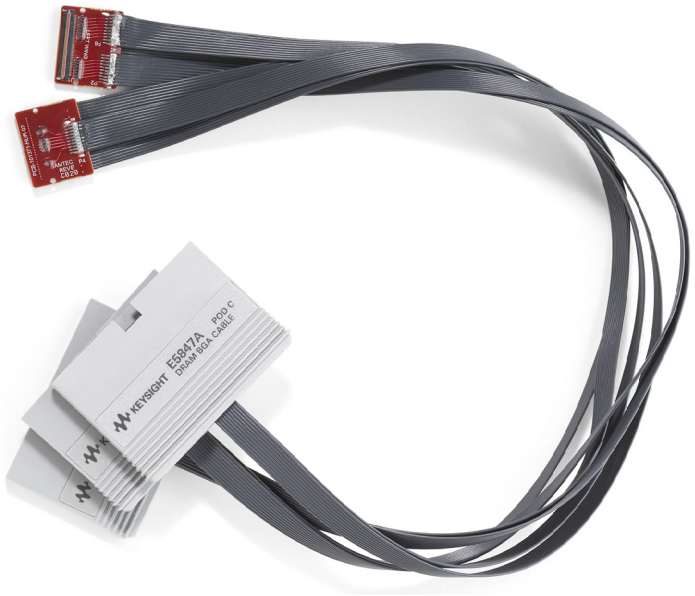
- W3635B scope adapters
- X-Series, V-Series, MXR-Series, or UXR-Series oscilloscopes
- Oscilloscope probes with probe heads

Use with logic analyzer requires

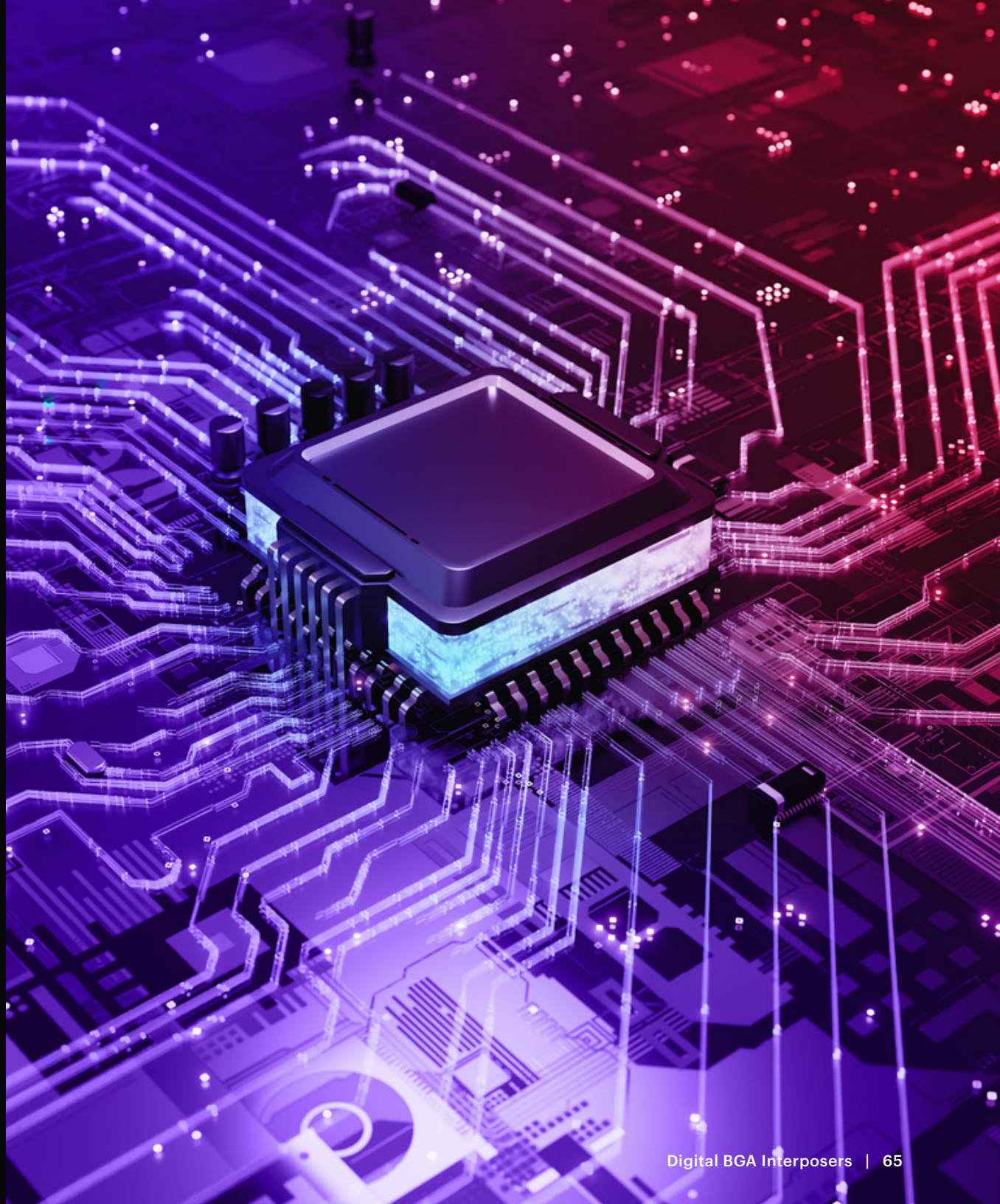
- Modified E5845A adapter cable
- U4164A module in AXIe chassis or 16864A logic analyzer
- Qty (2) U4201A logic analyzer cables
- M9537A embedded controller or host PC with PCI®e adapter card and PCI®e x8 cable, required for U4164A solution
- B4661A Memory Analysis software (base software for DDR Setup Assistant and default configurations)

Recommended

- B4661A Memory Analysis software licensed options:
  - B4661A-2TP/-2FP/-2NP DDR2/3/4 Listing Decoder
  - 4661A-3TP/3FP/3NP DDR2/3/4 and LPDDR2/3/4 Compliance Validation
  - B4661A-4TP/4FP/4NP DDR3/4, LPDDR2/3/4, and ONFi Analysis
- Memory depth option of choice for U4164A logic analyzer module



Additional Interposers

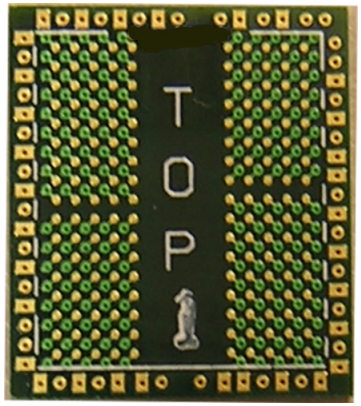


GDDR5 170 SIGNAL INTEGRITY INTERPOSER

Key features

- Enables correct operation of the GDDR5 interface while providing access to selected bus signals between the processor and LPDDR memory chip.
- Provides solder pads for use with Keysight E2677B or N5381A InfiniiMax single-ended / differential solder-in or Keysight N5425B ZIF probe head.
- Includes an S-parameter file to configure the oscilloscope to render waveforms as they exist at the DRAM pins.

Optimized for oscilloscope measurements, the GDDR5 170 BGA Interposer provides access to the GDDR signals and passes all power and ground signals between the processor and the memory chip.



Specifications

- Standard: GDDR5
- Ball count: 170
- DRAM size: 12 mm x 14 mm
- Optimized for oscilloscopes

Requires

- Solder-in differential probe heads
- InfiniiMax probe(s)
- Oscilloscope

	1	2	3	4	5		10	11	12	13	14	
A	VSSQ	DQ1	VSSQ	DQ0	VPP		VREFD	DQ8	VSSQ	DQ9	VSSQ	A
B	VDDQ	DQ3	VDDQ	DQ2	VSS		VSS	DQ10	VDDQ	DQ11	VDDQ	B
C	VSSQ	EDC0	VSSQ	VSSQ	VDD		VDD	VSSQ	VSSQ	EDC1	VSSQ	C
D	VDDQ	BDIO#	VDDQ	WCK01	WCK01#		VSS	VDD	VDDQ	DBI1#	VDDQ	D
E	VSSQ	DQ5	VSSQ	DQ4	VDDQ		VDDQ	DQ12	VSSQ	DQ13	VSSQ	E
F	VDDQ	DQ7	VDDQ	DQ6	VSSQ		VSSQ	DQ14	VDDQ	DQ15	VDDQ	F
G	VDD	VDDQ	RAS#	VDD	VSS		VSS	VDD	CS#	VDDQ	VDD	G
H	VSS	VSSQ	VDDQ	A10/A0	A9/A1		BA3/A3	BA0/A2	VDDQ	VSSQ	VSS	H
J	MF	RESET#	CKE#	ABI#	A12		SEN	CK#	CK	ZQ	VREFC	J
K	VSS	VSSQ	VDDQ	A8/A7	A11/A6		BA1/A5	BA2/A4	VDDQ	VSSQ	VSS	K
L	VDD	VDDQ	CAS#	VDD	VSS		VSS	VDD	WE#	VDDQ	VDD	L
M	VDDQ	DQ31	VDDQ	DQ30	VSSQ		VSSQ	DQ22	VDDQ	DQ23	VDDQ	M
N	VSSQ	DQ29	VSSQ	DQ28	VDDQ		VDDQ	DQ20	VSSQ	DQ21	VSSQ	N
P	VDDQ	DBI3#	VDDQ	WCK23	WCK23#		VSS	VDD	VDDQ	DBI2#	VDDQ	P
R	VSSQ	EDC3	VSSQ	VSSQ	VDD		VDD	VSSQ	VSSQ	EDC2	VSSQ	R
T	VDDQ	DQ27	VDDQ	DQ26	VSS		VSS	DQ18	VDDQ	DQ19	VDDQ	T
U	VSSQ	DQ25	VSSQ	DQ24	VPP		VREFD	DQ16	VSSQ	DQ17	VSSQ	U
	1	2	3	4	5		10	11	12	13	14	

eMMC 153 OR 169 BGA LOGIC ANALYZER INTERPOSER

Key features

- Provides connection to (address, command, control, and data) signals between a U4164A logic analysis system and eMMc 153-ball or 169-ball devices.
- Works with all solder finishes and tolerates lead-free soldering temperature profiles.a

The eMMC 153 or 169 ball logic analyzer Interposer is optimized for protocol measurements with a Keysight logic analyzer. It provides access to the highlighted signals and passes all power and ground signals between the processor and the memory chip.

Specifications

- Standard: eMMc
- Ball count: 153 or 169
- DRAM size: 11.5 mm x 11 mm
- Optimized for logic analyzers

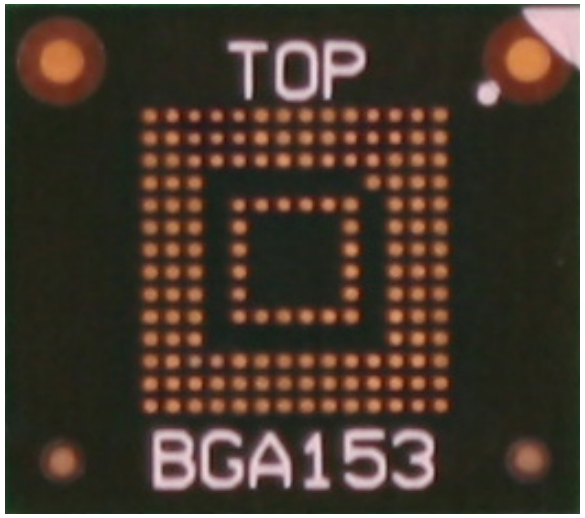
✹	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	NC	DAT0	DAT1	DAT2	RFU	RFU	NC	NC	NC	NC	NC	NC	NC	A
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC	B
C	NC	VDD	NC	GND	RFU	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC	C
D	NC	NC	NC	NC								NC	NC	NC	D
E	NC	NC	NC		RFU	VCC	GND	RFU	RFU	RFU		NC	NC	NC	E
F	NC	NC	NC		VCC					RFU		NC	NC	NC	F
G	NC	NC	RFU		GND					RFU		NC	NC	NC	G
H	NC	NC	NC		DSTRB					GND		NC	NC	NC	H
J	NC	NC	NC		RFU					VCC		NC	NC	NC	J
K	NC	NC	NC		RSTN	RFU	RFU	GND	VCC	RFU		NC	NC	NC	K
L	NC	NC	NC									NC	NC	NC	L
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC	M
N	NC	GND	NC	VCCQ	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	N
P	NC	NC	VCCQ	GND	VCCQ	GND	RFU	NC	NC	RFU	NC	NC	NC	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

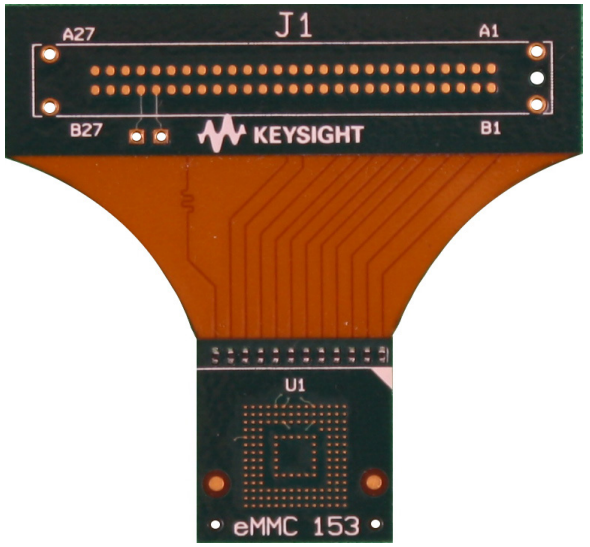
Requires

- Qty (1) E5406A soft touch pro probe
- Qty (2) U4201A logic analyzer cables
- Qty (1) U4164A module in AXIe chassis or 16864A logic analyzer
- M9537A embedded controller or host PC with PCI®e adapter card and PCI®e x8 cable, required for U4164A solution

Recommended

- Memory depth option of choice for U4164A logic analyzer module





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